20th International Workshop on Microprocessor and SOC Test, Security and Verification Final Program

December 9-10, 2019
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
http://mtvcon.org
General Chair: Magdy Abadir (Abadir & Associates)
Vice-General Co-Chair: Li-C. Wang (University of California at Santa Barbara)
Vice-General Co-Chair: Jayanta Bhadra (AMD)
Program Co-Chair: Wen Chen (NXP)
Program Co-Chair: Xiao (Sean) Sun (NXP)
Security Track Co-Chair: Sohrab Aftabjahani (Intel)
Security Track Co-Chair: Sandip Ray (Univ. of Florida)

Monday December 9, 2019

7:30-8:00 am: Registration and Cont. breakfast

8:00- 9:20am MTV Plenary Session
Opening Remarks: General Chair - Magdy Abadir

Keynote Speaker: Susheel Tadikonda, Vice President of Verification Continuum Solutions Engineering (Synopsys)
Title: AI on the Edge–The Future of Computing

Keynote Speaker: Jacob Abraham, Professor and Director of the Computer Engineering Research Center (UT-Austin)
Title: Extending the Capacity of Verification Tools

9:20 – 10:00 am - Session A: Machine Learning
Session Chair: Atefeh Einafshar (Intel)

Instant Automatic Debug, Markus Borg (RISE SICS AB), Oscar Werneman, Daniel Hansson (Verifyter), Ali Parsai (University of Antwerp)

Expediting Design Bug Discovery in Regressions of x86 processors Using Machine Learning, Ahmed Wahba, Justin Hohnerlein, Farhan Rahman (AMD)

10:00-10:15 am - Coffee Break

10:15-10:55 am - Session B: SoC and System level Security Assurance
Session Chair: Navid Asadi (Univ. of Florida)

System-level security verification using commercial simulation and emulation environments, Jason Oberg, PhD, CEO (Tortuga Logic)

Exploration for enhancing security assurance in SoC's
Brent Thomas, Principle Engineer (Intel)

10:55 - 12:00 pm – PANEL 1: Security of Artificial Intelligence Systems
Organizer: Sohrab Aftabjahani, Ph.D. (Intel)
Moderator: Sandip Ray, Professor (U of Florida)
Panelists:

- Michael Borza, Security Technologist (Synopsys)
- Swaroop Ghosh, Assistant Prof. (Penn St Univ.)
- Nicole Fern, Sr. HW Security Eng.(Tortuga Logic)
- Sohrab Aftabjahani, Ph.D. (Intel)

12:00 - 1:00 pm – Lunch

1:00 – 2:00 pm – Session C: Machine Learning
Session Chair: Wen Chen (NXP)

Building safe and intelligent autonomous driving systems out of silicon and software blocks, Colin , Cureton, Sr. Dir of ADAS Product Management (NXP)

Machine Learning-Based Hotspot Detection: Fallacies, Pitfalls, and Marching Orders
Gaurav Rajavendra Reddy, Kareem Madkour and Yiorgos Makris (Univ. of Texas Dallas)

Plot-Based Analytics for Production and Test Data
Jay Shan (IE3A Inc) and Li C. Wang (UCSB)

2:00 – 2:20 Invited Talk
Session Chair: Adam Abadir (AMD)
Using Simulation Acceleration to Speed Block and Platform Level IP Verification, Hillel Miller (Synopsys)

2:20 - 3:20 pm - Session D: Industrial Processor Verification & Validation
Session Chair: Adam Abadir (AMD)

Post-silicon validation of MMU in POWER9 Chip, Shay Aviv (IBM- Haifa)

Open-source Validation Suite for RISC-V
Mikhail Chupilko, Alexander Kamkin, Alexander Protsenko (ISP RAS)

A verification Framework of Neural Processing Unit for super resolution

Jinsae Jung, Jaeun Park, Apurva Kumar (Samsung)

3:20-3:35 pm - Break

3:35-4:55 pm - Session E: Security Validation Tools and Methodologies
Session Chair: Sohrab Aftabjahani (Intel)

Backside Security Assessment of Modern SoCs
Mir Tanjidur Rahman, Navid Asadi (U of Florida)

On the Detection of Always-on Hardware Trojans Annachiara Ruospo, Ernesto Sanchez (Poli di Torino)

Pre-silicon graphics hardware fuzzing approach to find security vulnerabilities
Vyasa Sai, Carlos Arias (Intel)

Fault injection attack and a study of simulation tool
Zongyao Wen (Synopsys)

4:55 – 5:55 pm - Session F: Methodology Innovations
Session Chair: Marco Cantu (Ericson)

Wafer Level Burn-In: A New Reliability Stress Methodology for Automotive Microcontrollers
Chen He, Yanyao Yu (NXP)

Disk space management techniques for Silicon Engineers, Jigar Savla (Georgia Inst. of Technology)

6:45 pm - MTV Workshop Gala Dinner at *Fogo de Chão,* 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220. Fogo de Chão is an authentic Brazilian steakhouse offering an incredible selection of grilled meats, salads and fresh vegetable. Restaurant is a short walk ~12 minutes from the Hyatt, or take a short taxi. fogodechao.com/locations/austin/

Tuesday December 10, 2019

7:30-8:00 am - Registration and cont. breakfast

8:00-9:00 am - Session G: Formal/Semi-Formal Verification
Session Chair: Vivek Vedula (ARM)

Sequential Equivalence Checking Beyond Clock Gating
Xiushan Feng (Samsung), Sudipta Kundu, Mitesh Jain, David Lee Xiaolin Chen (Synopsys)

Hardware/Software Co-verification Using Path-based Symbolic Execution
Rajdeep Mukherjee (Cadence), Saurabh Joshi (IIT Hyderabad), John O'leary (Intel), Daniel Kroening (University of Oxford), Tom Melham (University of Oxford)

How to Use Formal Analysis to Prevent Deadlocks
Jeremy Levitt, Ping Yeung, and Mark Eslinger (Mentor, A Siemens Business)

9:00-9:15 am - Coffee Break

9:15 – 10:15 am - Session H: Stimulus Generation & Design Verification considerations
Session Chair: Amir Daneshbeh (Ericson)

Automated SystemC Test Generation using Search-based Testing and Concolic Testing
Mustafa Efendioglu, Alper Sen (Bogazici University)

Coverage Directed Generation Using Optimization Techniques and Approximated Targets
Ziv Nevo Raviv Gal, Avi Ziv (IBM Research - Haifa)

RamGen: Moving Memory from Physical to the Logical domain
Jeff Scott, Jonathan Sadowsky (Juniper Networks), and Jigar Savla (Georgia Inst. Of Tech.)

10:15 – 10:35 am: SVDTC Standard Update, Debug Sub-committee
Session Chair: Magdy Abadir

Techniques for Debug of Low Power SoCs
Sankaran Menon[1], Chinna Prudvi[1], Rolf Kuehnis[1], Sukhbinder Singh Takhar[1], Spencer Millican[2], Eric Rentschler[3], Pandy Kalimuthu[4], Preeti Ranjan Panda[5], Priyadarsan Patra[6], Ashish Gupta[7]
[1] Intel Corporation, [2]Auburn University, [3]Mentor Graphics (A Siemens Business), [4]Texas Instruments, [5]IIT Delhi, India, [6]Xavier University, Bhubaneswar, India, [7]NXP, India.

10:35- 11:45 pm PANEL 2: Beyond the Bounds of Research: Machine Learning meets Design Automation
Organizer: Harry Foster (Mentor, Siemens Bus.)
Moderator: Duaine Pryor, PhD Chief Technologist (Mentor, Siemens Business)
Panelists:

- Monica Farkash, PhD, Principal Member of Technical Staff (AMD)
- Daniel Hansson, Founder & CEO (Verifyter)
- Mark Conklin, Principal Engineer (ARM)
- Madhu Rangarajan, Sr Principal Engineer (Intel)
- Sean Sun, Director of Engineering (NXP)

11:45-12:45 pm - Lunch

12:45 – 1:45 pm - Session I: Hardware and System Security Trends and Standards
Session Chair: Xiao (Sean) Sun (NXP)

On-Chip Security Implementations
Brandon Wang, VP, Strategic Directions, Synopsys

Hardware and Software Co-Verification from Security Perspective, Jun Ke (Northeastern Univ.), Yumin Hou, Yier Jin (U. of Florida) & Xiaolong Guo (Kansas St. U)

A Path to IP Security Assurance Standard
Brent Sherman (Intel), Sohrab Aftabjahani (Intel), Ireneusz Sobanski (Intel), Mike Borza (Synopsys), Anders Nordstrom (Synopsys), Adam Sherer (Cadence), James Pangburn (Cadence), Ambar Sarkar (NVIDIA), Wen Chen (NXP), Kathy Herring Hayashi (Qualcomm), Sridhar Nimmagadda (Qualcomm), Michael Munsey (Methodics), John Hallman (OneSpin Solutions), Alric Althoff (Leidos), and Jonathan Valamehr (Tortuga Logic)

1:45 – 3:05 pm – Session J: Innovative Hardware Security Solutions
Session Chair: Ahmed Wahba (AMD)

TrappeD: Assessing eDRAM/DRAM Trojans and Countermeasures for Information Leakage and Fault Injection, Swaroop Ghosh (Penn State University)

Multilayer camouflaged secure boot for SoCs
Ali Shuja Siddiqui, Yutian Gui, and Fareena Saqib (University of North Carolina Charlotte)

How real are hardware security bugs?, JV Rajendran, Associate Professor (Texas A&M University)

Using Fault Simulation for Measuring Resistance to Malicious Fault Attacks on Security HW
Brian Davenport (Synopsys)

3:05 - 3:20 pm - Break

3:20 - 4:20 pm - Session K: Functional Safety, Test Selection and Reuse
Session Chair: Alper Sen (Bogazici Univ. Turkey)

A more efficient approach to ASIL B compliance of a Microprocessor, Bryan Ramirez and Terry Lyons (Mentor, A Siemens Business)

Effective Reuse through Virtual Platforms, Glenn Canto (Ericson, Austin)

Automated Test Picker for Complex Microprocessor Verification Environment
Chetas Mapara, Jerrin Jose (AMD)

4:20 - 5:20pm - Session M: Performance and Architectural Verification
Session Chair: Himyanshu Anand (Nvidia)

Case Study: SoC Performance Verification and Static Verification of RTL Parameters
Prokash Ghosh, Rohit Srivastava (NXP Semiconductors India Pvt Ltd)

Design Crawler: A Web Application for Digital Design Metadata Analysis
Sherif Hosny (Mentor Graphics), Amr Baher (Mentor Graphics)

Data Collection, Modelling & Analysis for Performance measurement in a multi-master framework, Manish Kumar Agarwal, Amandeep Sharan, Mohammad Asif Khan, Atul Gupta (NXP semiconductors)

5:20 pm - Closing Remarks , Magdy Abadir

MTV 2019 Corporate Supporters

Diamond Supporter

Synopsys®
Silicon to Software™

Platinum Supporter

IBM

Gold Supporter

Mentor®
A Siemens Business

Silver Supporters

AMD

ARM

ERICSSON

intel®

NXP

SAMSUNG