



16th International Workshop on Microprocessor and SOC Test and Verification

Advance Program
December 3-4, 2015

Hyatt Regency Hotel on Town Lake, Austin, Texas
<http://mtvcon.org>

General Chair: Magdy Abadir
Program Co-Chair: Jay Bhadra (Freescale)
Program Co-Chair: Li-C. Wang (UCSB)
Vice Program Chair: Wen Chen (Freescale)

MTV 2015 Corporate Supporters

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Preliminary Activities

December 2, 2015:

Venue: Norris Conference Center, 2525 W
Anderson Ln #365, Austin, TX 78757
Joint Event with DVClub of Austin

Agenda:

11:30 am: Doors Open / Networking

12:00 -1:00 pm: Lunch and Presentation:

"I Created the Verification Gap"

*Ram Narayan and Tom Symons, Oracle Labs,
Austin, Texas*

1:00 - 1:15 pm: Networking

1:15 - 2:15 pm: MTV Tutorial

**"Virtual Platform technology for ESL Design
and Verification"**

*Instructors: Magdy El-Moursy and Ashraf
Salem, Mentor Graphics, Egypt*

Technical Program

December 3, 2015

7:30-8:00 am: Registration and continental
breakfast

8:00 -8:10 am Opening Remarks
Magdy Abadir, MTV General Chair

8:10-8:55 am Keynote Speaker
Li C Wang (University of California at Santa
Barbara)

*Big Data Analytics for Validation and Test - Big
Opportunities and Big Challenges*

8:55-9:55 am - Session A. Test Generation Techniques

Session Chair: Daniela Tenova (Altera)

A.1 Specification-Based Test Program Generation for ARM VMSAv8-64 Memory Management Units

Mikhail Chupilko, Alexander Kamkin, Artem Kotsynyak, Alexander Protsenko, Sergey Smolov and Andrei Tatarnikov (ISP RAS, Russia)

A.2 Enhancing the capability of constrained random test program generators via learning and test filtering

Vinayak Kamath (AMD)

A.3 Is Your Testing N-wise or Unwise? Pairwise and N-wise Patterns in System Verilog for Efficient Test Configuration and Stimulus

Jonathan Bromley and Kevin Johnston (Verilab)

9:55-10:15 am - Coffee Break

10:15-10:55 am - Session B. Metric Driven Verification

Session Chair: Ashraf Salem (Mentor)

B.1 Enhancing the stress and efficiency of RIS tools using coverage metrics

Gunaranjan Kurucheti and John Hudson (ARM)

B.2 The Challenges of Automatic Coverage Closure

Marat Teplitsky & Amit Metodi (Cadence, Israel)

11:00 am -12:00 pm - PANEL 1: AMS Verification Challenges

Organizer: Jay Bhadra (Freescale)

Moderator: Abhishek Kumar (Freescale)

Panelists:

1. Peng Li (Texas A&M)
2. Abhijit Chatterjee (Georgia Tech)
3. Duaine Pryor (Mentor)
4. Noam Teutsch (TI)
5. Senthil Vinayagam (Cobham)

12:00-1:30 pm Lunch

1:30-2:30 pm - Session C. Leveraging Virtual Models and Emulation

Session Chair: Adam Abadir (AMD)

C.1 SoC Development and Prototype with VDK

Taylor Holmes, Andrew Passerelli and John Connor (Northrop Grumman)

C.2 Leveraging Virtual Prototype Models for Hardware Verification of an Accelerated Network Packet Processing Engine

Sourav Roy, Nikhil Jain, Sandeep Jain and Robert Page (Freescale)

C.3 Verification of a Cache Coherent system with an A53 cluster using ACE VIP with Graph Based Stimulus

Perry Wobil and Galen Blake (Altera)

2:30 - 3:30 pm - Panel 2 Emulation as a mainstream verification methodology: benefits and practical considerations.

Organizers: Farhan Rahman (AMD) and Magdy Abadir

Moderator: Farhan Rahman (AMD)

Panelists:

1. Susheel Tadikonda (Synopsys)
 2. Stephen Bailey (Mentor)
 3. William Hodges (Intel)
 4. Rob Oshana (Freescale)
 5. David Bural (TI)
 6. Mark LaVine (ARM)
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Break 3:30-3:45pm

3:45-4:45 pm - Session D. Debug and Test Coverage

Session Chair: Jayanta Bhadra (Freescale)

D.1 *A Topological Approach to Hardware Bug Triage*

Rico Angell, Andrew Deorio and Ben Oztalay
(University of Michigan)

D.2 *Automatic Bug Fixing*

Daniel Hansson (Verifyter, Sweden)

D.3 *Novel MC/DC Coverage Test Sets Generation Algorithm, and MC/DC Design Fault Detection Strength Insights*

Mohamed Salem and Kerstin Eder (University of Bristol, UK), Presented by Harry Foster (Mentor)

6:00pm - MTV Workshop Dinner

Venue: *Fogo de Chão*, 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220.

Fogo de Chão is an authentic Brazilian steakhouse.

<http://www.fogodechao.com/locations/austin/>

Transportation: No transportation is provided. Attendees can have a short walk ~10-15 minutes from the Hyatt to the restaurant, or take a short taxi.



December 4, 2015

7:30-8:00am - Registration & cont. breakfast

8:00-8:20 am Invited Talk: *Meeting the RAS verification challenge: IBM's perspective on verifying design reliability.* **Shiri Moran (IBM)**

8:20-9:20am – PANEL 3: Portable Stimulus and Testbenches – Possibilities or Wishful Thinking?

Organizers: Harry Foster (Mentor Graphics) and Jay Bhadra (Freescale)

Moderator: Harry Foster (Mentor Graphics)

Panelists:

1. Monica Farkash (Freescale)
2. Tom Anderson (Breker)
3. Tom Fitzpatrick (Mentor)
4. Mike Stellfox (Cadence)
5. Daniel Schostak (ARM)
6. Hillel Miller (Synopsys)

9:20-9:40 am Invited Talk: *TransLight: a lightning-fast solution for handling complex address translation mechanisms in post-silicon exercisers*

Anatoly Koyfman (IBM)

9:40-10:00 am Coffee Break

10:00-11:00 am - Special session:

Security Verification Part 1

Organizer: Mark Tehranipoor (University of Florida)

Session Chair: Wen Chen (Freescale)

S1.1 *Harnessing Nanoscale Device Properties for Hardware Security*

Bicky Shakya, Fahim Rahman, Mark Tehranipoor and Domenic Forte (University of Florida)

S1.2 *Hierarchy-Preserving Formal Verification Methods for Pre-Silicon Security Assurance*

Xiaolong Guo, Raj Gautam Dutta and Yier Jin (University of Central Florida)

S1.3 *Hardware-Intrinsic Security based on Physical Unclonable Functions*

Michael Orshansky (University of Texas at Austin)

**11:00 am-12:00 pm - Special session:
Security Verification part 2**
Organizers: J. Bhadra & W Chen (Freescale)
Session Chair: Mark Lavine (ARM)

S2.1 *Using an FPGA as a Gateway Tester for Enhanced Security in 3D Stacked ICs*

Jennifer L. Dworak, Al Crouch, Kundan Nepal and John Potter (Southern Methodist Univ, SiliconAid, Univ. of St. Thomas, ASSET InterTech)

S2.2 *Verifying Hardware Security Properties*
Jason Oberg (Tortuga Logic)

S2.3 *Security Beyond Checklist Compliance*
Mohit Arora (Freescale)

12:00-1:15 pm Lunch

1:15-1:55 pm - Session E. Formal Techniques
Session Chair: Hillel Miller (Synopsys)

E.1 *Reset IP Verification Signoff with Formal*
Xiaolin Chen and Baosheng Wang (Synopsys, AMD)

E.2 *A Vendor-Independent Formal Unreachability Analysis Flow for Automated Coverage Closure*
Xiushan Feng, Abhishek Muchandikar, Sunil Keerthi and Praveen Tiwari (Nvidia)

**1:55 - 2:55 pm - Special session:
Security and Verification part 3**
Session Chair: Daniela Toneva (Altera)

S3.1 *Design for Security and Secure Supply Chain Enablement*
Tom Katsioulas (Mentor Graphics)

S3.2 *Basic Models for Microprocessor Security*
Peter-Michael Seidel and Mark Nelson
(University of Hawaii at Manoa)

S3.3 *Modeling and Analysis of Trusted Boot Processes based on Actor Network Procedures*
Peter-Michael Seidel and Mark Nelson
(University of Hawaii at Manoa)

2:55-3:10pm Break

3:10-3:50 pm - Session F. Performance Characterization/Verification
Session Chair: Jennifer Dworak (SMU)

F.1 *Performance of a SystemVerilog Sudoku Solver with VCS*
Jeremy Ridgeway (Avago)

F.2 *Characterizing Processors for Energy and Performance Management*
Harshit Goyal and Vishwani Agrawal (Auburn University)

3:50 - 4:50 pm Session G. Methodology Innovations
Session Chair: Xiao Sun (Freescale)

G.1 *Correct Runtime Operation for NoCs through Adaptive-Region Protection*
Rawan Abdel-Khalek and Valeria Bertacco
(University of Michigan)

G.2 *Mastering Reactive Slaves in UVM*
Jeffrey Montesano, Mark Litterick and Taruna Reddy (Verilab)

G.3 *SOC Verification using Portable Test and Stimulus Descriptions*
Sharon Rosenberg, Larry Melling and John Nehls (Cadence)

4:50-5:00 pm Closing Remarks
Magdy Abadir

