



**19th International Workshop on  
Microprocessor/SOC Test, Security &  
Verification  
Final Program**

December 10-11, 2018  
Hyatt Regency Hotel, Austin, Texas, USA  
<http://mtvcon.org>

General Chair: Magdy Abadir (Helic)  
Vice-General co-Chair: Li-C. Wang (UCSB)  
Vice-General Co-Chair: Jay Bhadra (AMD)  
Program Co-Chair: Wen Chen (NXP)  
Program Co-Chair: Xiao (Sean) Sun (NXP)  
Security Track Co-Chair: Sohrab Aftabjahani (Intel)  
Security Track Co-Chair: Sandip Ray (U. of Florida)

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**Monday December 10, 2018**

**7:30-8:00am: Registration and cont. breakfast**

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**8:00 – 8:45 MTV Plenary Session**

**Opening Remarks: General Chair - Magdy Abadir (Helic)**

**Keynote Speaker: Vikas Gautam, VP of R&D, Functional Safety (Synopsys)**

**Title: Future of Functional Safety: Going beyond ISO 26262 to enable scaling verification for next-generation automotive SoC designs**

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**8:45-10:05 am - Session A. Functional Safety**

**Session Chair: Neeta Ganguly (Intel)**

**A.1 Proving the capability of Arm IP for functional safety applications**  
Asif Jafri (ARM)

**A.2 Accelerating ISO 26262 Functional Safety Development with Mentor Safe IC**  
Terry Lyons and Sanjay Pillay (Mentor, A Siemens Business)

**A.3 Back to the future: Fault injection – State of the Art practices**  
Brian Davenport (Synopsys)

**A.4 Addressing the Challenges of IP Functional Safety Analysis – An Insider's View**  
Ghani Kanawati (ARM)

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**10:05-10:20 am Coffee Break**

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**10:20-11:00 am - Session B. Stimulus Generation**  
**Session Chair: Wen Chen (NXP)**

**B.1 Test Program Generator MicroTESK for RISC-V**  
Mikhail Chupilko, Alexander Kamkin, Artem Kotsynnyak, Alexander Protsenko, Sergey Smolov (ISP RAS), and Andrei Tatarnikov (HSE)

**B.2 Fast Reliable Verification Methodology for RISC-V without a Reference Model**  
Abdelfattah Munir (Information Technology Institute), Samer Ahmed (Valeo,Egypt), Mina Magdy (Mentor, Egypt), Sameh El-Ashry (Si-Vision,Egypt), Ahmed Shalaby (Benha University, Egypt)

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**11:00-12:00 pm – PANEL: The Road to Functional Safety—Are We There Yet?**

**Organizer and Moderator: Harry Foster (Mentor, Siemens Business)**

**Panelists:**

Sanjay Pillay (Mentor, Siemens Business)  
Vikas Gautam (VP R&D Functional Safety Synopsys)  
Ghani Kanawati (Functional Safety Mgr Lead, ARM)  
Mathieu Blazy-Winning (Functional Safety Mgr, NXP)

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**12:00 - 1:00 pm - Lunch**

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**1:00-1:30 pm – Keynote Speaker: Prof. Swarup Bhunia, Univ. of Florida**  
**Title: Verification of “Things”: From Microchip to Medicine**

**Session Chair: Magdy Abadir (Helic)**

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**1:30 – 2:00 Distinguished Speaker: Amitabh Das (AMD)**

**Title: Analysis, Design & Implementation of Nonce-Misuse Resistant Authenticated Encryption Schemes**

**Session Chair: Sohrab Aftabjahani (Intel)**

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**2:00-3:00 pm Session D. Security Innovations**  
**Session Chair: Daniela Toneva (Ericsson)**

**D.1 Mining Security Critical Linear Temporal Logic Specifications for Processors**  
Calvin Deutschbein and Cynthia Sturton (The University of North Carolina at Chapel Hill)

**D.2 A Novel Approach in Security Verification using Fault Injection Method**  
Boon Pin Liong, Amir Daneshbeh, and Ilyas Bin Abdul Rahman (Intel)

**D.3 A Perceptron-Inspired Technique for Hardware Obfuscation**  
Siroos Madani, Mohammad R Madani, and Magdy Bayoumi (University of Louisiana at Lafayette)

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**3:00-3:15 pm - Break**

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**3:15-4:15 pm - PANEL Security Validation: Trends and Challenges**

**Organizer: Sandip Ray (Univ of Florida)**

**Moderator: Sohrab Aftabjahani (Intel)**

**Panelists:**

David Kaplan (Security Architecture Fellow, AMD)  
Jason Oberg (CEO, Tortuga Logic)  
Claire Vishik (Sr. Director, Global Trusted Sys., Intel)  
Zongyao Wen (Director of Verification, Synopsys)

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**4:15-5:15 pm - Session E. Coverage, and Data Analysis**

**Session Chair: Atefeh Einafshar (Intel)**

**E.1 How to close coverage 10x faster using Portable Stimulus Standard – A case study**  
Shelly Henry and Nirabh Regmi (Microsoft)

**E.2 Schmoos data analysis using Machine Language Algorithms**  
Rekha Bangalore, Adeosun Oluwatosin, Kelvin Lam (Intel)

**E.3 Application of Combinatorial Test (CT) for Product Validation**  
Rekha Bangalore and Raji Bandanapudi (Intel)

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**6:30pm - MTV Workshop Gala Dinner**

**Venue: Fogo de Chão, 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220.**

Fogo de Chão is an authentic Brazilian steakhouse offering an incredible selection of grilled meats, salads and fresh vegetable. Please visit <http://www.fogodechao.com/locations/austin/>

**Transportation:** short walk ~12 minutes from the Hyatt to the restaurant, or take a short taxi

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## **Tuesday December 11, 2018**

**7:30-8:00 am - Registration and continental breakfast**

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**8:00-8:30 am Keynote Speaker: Prof. Li C Wang (IEEE Fellow, Univ. of California at Santa Barbara)**

**Title: The Hype and Fear of AI - Introduction to Intelligent Engineering Assistant (IEA)**

**Session Chair: Magdy Abadir (Helic)**

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**8:30-9:30 am - Session F. Machine Learning**

**Session Chair: Wen Chen (NXP)**

**F.1 Predicting Buggy Modules During Virtual Prototype Development**  
Mustafa Efendioglu, Alper Sen, and Yavuz Koroglu (Bogazici University),

**F.2 Boosting Continuous Integration performance with Machine Learning**  
Christian Graber, Daniel Hansson (Verifyter), and Adam Tornhill (Empear)

**F.3 Mining version control data - are software and hardware the same?**  
Raviv Gal, Rachel Tzoref-Brill and Avi Ziv (IBM Research - Haifa)

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**9:30-9:45 am - Coffee Break**

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**9:45 – 10:45 Session G Formal & Validation****Session Chair: Adam Abadir (AMD)**

**G.1** Catching X-Propagation RTL Bugs through Formal Verification  
Xiushan Feng (Samsung)

**G.2** High Speed Input Output (HSIO) Test Automation and Standardization Using the Origen-SDK Open Source Platform  
Shane Sanders and Brian Caquelin (AMD)

**G.3** Multi-master validation framework for next generation automotive SOCs  
Manish Kumar Agarwal, Amandeep Sharan, Mohammad Asif Khan, Atul Gupta (NXP)

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**10:45-11:45 am - Session H: FPGA and Emulation****Session Chair: Sean Sun (NXP)**

**H.1** 2018 FPGA Functional Verification Trends  
Harry Foster (Mentor, A Siemens Business)

**H.2** A UVM Based Emulation Friendly SoC Verification Environment  
Weihua Han and Hillel Miller (Synopsys)

**H.3** Getting started on Co-Emulation,  
Jigar Savla (Juniper Networks)

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**11:45 am – 1:00 pm - Lunch**

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**1:00 – 2:00 pm – Distinguished Talks****Session Chair: Sean Sun (NXP)**

Techniques for Analog IP Protection  
Prof. Jiang Hu, IEEE fellow (Texas A&M University)

Reducing the risk of Electromagnetic Coupling in Complex SOC Designs  
Dr. Yorgos Koutsoyannopolous (Helic)

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**2:00 – 3:20 pm – Session I: Quality Analysis and Post-Silicon Validation****Session Chair: Monica Farkash (NXP)**

**I.1** Deeper Quality Analysis with Template-Aware Coverage (TAC)  
Raviv Gal, Anatoly Koyfman and Avi Ziv (IBM Israel)

**I.2** Automatic Debug Quantification for Workload Balance and Progress Tracking  
Yanhua Cao, Osama Shoubber, Pallavi Jesrani (AMD)

**I.3** Advanced Regression Management for Post-Silicon Validation of Automotive SOCs  
Ayushi Agarwal, Pankaj Gupta, and Atul Gupta (NXP)

**I.4** POWER9 post silicon validation using the Threadmill exerciser  
Hillel Mendelson, Tom Kolan, Vitali Sokhin (IBM-Israel)

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**3:20-3:40 pm - Break**

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**3:40 – 5:20 pm - Session J. Test Bench and simulation Innovations****Session Chair: Avi Ziv (IBM)**

**J.1** Portable Stimulus Standard for Practical Applications  
Swami Venkatesan, Steve Brown and Sharon Rosenberg (Cadence)

**J.2** Efficient Methodology of Sampling UVM RAL during Simulation for SoC Functional Coverage  
Sameh Elashry and Ahmed Adel (Si-Vision)

**J.3** Different Reference Models for UVM Environment to Speed Up the Verification Time  
Amr Moursi, Romaisaa Samhoud (Mentor A Siemens Business), Yaseen Kamal, Mazen Magdy (Alexandria University, Egypt), Sameh El-Ashry (Ain Shams Univ., Egypt.), Ahmed Shalaby (Benha Univ. Egypt)

**J.4** Transaction based speedup for simulation replay  
Priti Nagarajan (Advanced Micro Devices), Chetas Mapara (Advanced Micro Devices),

**J.5** Pre-Silicon DFT verification on SOC slim model  
Archana Rengaraj and Pratheema Mohandoss (Intel)

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**5:20 - 5:30 pm Closing Remarks – Magdy Abadir**

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