18th International Workshop on Microprocessor and SOC Test, Security and Verification Final Program

December 11-12, 2017
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
http://mtvcon.org

General Chair: Magdy Abadir (Helic)
Vice-General Chair: Li-C. Wang (University of California at Santa Barbara)
Program Co-Chair: Jay Bhadra (NXP)
Program Co-Chair: Xiao (Sean) Sun (NXP)
Security Track Co-Chair: Sohrab Aftabjahani (Intel)
Security Track Co-Chair: Sandip Ray (NXP)
Vice Program Chair: Wen Chen (NXP)

Monday December 11, 2017

7:30-8:00am: Registration and cont. breakfast

8:00 – 9:10 MTV Plenary Session
Opening Remarks: General Chair - Magdy Abadir (Helic)

Keynote Speaker 1: Kamal Khouri, VP Autonomous Driving, Automotive (NXP)
Title: ***The Future of Automotive: Verification Challenges and Solutions***

Keynote Speaker 2: **Mike Goddard, Sr. VP (Samsung Austin R&D Center)**
Title: "The Evolving Verification Role of Complex CPU and System IP"
Organized by Synopsys

9:10-10:10 am - Session A. Test Generation for Processor Verification
Session Chair: Avi Ziv (IBM)

A.1 *Anvil: Best in Class Multiprocessor Coherency Verification Tool*
Kaushik Gopalakrishnan and Bipin Ravi (ARM)
A.2 *Dynamic Exerciser Template Weighting in x86 Processor Verification,*

Ahmed Wahba (UC Santa Barbara), Justin Hohnerlein, Farhan Rahman (AMD), and Li-C. Wang (UC Santa Barbara)
A.3 *Maintaining ISA Specifications in the MicroTESK Test Program Generator*
Andrei Tatarnikov, Mikhail Chupilko Alexander Kamkin, Alexander Protsenko Artem Kotsynyak, and Sergey Smolov (ISP RAS, Russia)

10:10-10:30 am Coffee Break

10:30-11:30 am - Session B. Multicore and Architectural Verification
Session Chair: Farhan Raman (AMD)

B.1 *Sequence Language: A Constraint Random MP-RIS Generation Framework*, Madhukarreddy Pappireddy and Bipin Ravi (ARM)
B.2 *Validation of Context Preserving Thread-Level Speculative Execution: Comparison of Non-TLS and CPSE-enabled Applications*
Jack Mason (Nova Southeastern University)
B.3 *IDeALS – Intelligent Detection and Accurate Localization of Stalls,* Pallavi Jesrani (AMD)

11:30 am-12:00 pm – Distinguished Speaker: Neil Stroud, Director (ARM)
Title: Functional Safety
Session Chair: Xiao (Sean) Sun (NXP)

12:00-1:00 pm - Lunch

1:00-1:30 pm - Keynote Speaker 3: Yier Jin, IoT Embedded Professor (Univ of Florida)
Title*:* Hardware Supported Cybersecurity for IoT
Session Chair: Sohrab Aftabjahani (Intel)

1:30-2:30 pm Session C. Security-Aware Design Innovations
Session Chair: Jason Oberg (Tortuga Logic)

C.1 *A Security-Aware Pre-partitioning Technique for 3D Integrated Circuits*
Siroos Madani and Magdy Bayoumi (University of Louisiana)
C.2 *iPUF: Interconnect PUF with Self-Masking Circuit for Performance Enhancement*
Xiaoxiao Wang, Liting Yu (Beihang University, China), Fahim Rahman, and Mark Tehranipoor (University of Florida)
C.3 *Modeling and Analysis of Secure Processor Extensions based on Actor Network Procedures*
Mark Nelson and Peter-Michael Seidel (University of Hawaii at Manoa)

2:30-2:50 pm – Distinguished Speaker: Richard Soja (NXP)
Title: Automotive Security – Introduction
Session Chair: Li C Wang (UCSB)

2:50-3:10 pm - Break

3:10-4:10 pm - PANEL 1
Title: Trends and Challenges in Security Validation of SoC's
Organizer & Moderator: Sohrab Aftabjahani (Intel)
Panelists:

1. Lawrence Loh (Cadence)
2. Anders Nordstrom (Synopsys, Canada)
3. Harry Foster (Siemens/Mentor)
4. Jason Oberg (Tortuga Logic)
5. Siddharth Garg (New York University)

4:10-5:30 pm - Session D. Security and Trust
Session Chair: Sandip Ray (NXP)
D.1 *Mutual Authentication: A Robust Solution for Preventing System-Level Cloning*
Ujjwal Guin (Auburn University)
D.2 *Validation of EM Side-Channel Attack Resilience*
Michael Orshansky (University of Texas at Austin)
D.3 *Rethinking Instruction-Set Guarantees for Software-Driven Hardware Security*
Ashay Rane, Calvin Lin and Mohit Tiwari (University of Texas at Austin)
D.4 *Identifying and Measuring Security Critical Path for Uncovering Circuit Vulnerabilities*
Wei Hu and Ryan Kastner (Northwestern Polytechnical University, China)

6:30pm - MTV Workshop Gala Dinner
Venue: *Fogo de Chão,* 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220.
Fogo de Chão is an authentic Brazilian steakhouse offering an incredible selection of grilled meats, salads and fresh vegetable. Please visit http://www.fogodechao.com/locations/austin/
Transportation: short walk ~12 minutes from the Hyatt to the restaurant, or take a short taxi

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Tuesday December 12, 2017

7:30-8:00 am - Registration and continental breakfast

8:00-8:30 am Distinguished Speaker: Avi Ziv (IBM Research - Haifa Israel)
Coverage Directed Generation – Past, Present, and Future
Session Chair: Magdy Abadir (Helic)

8:30-9:50 am - Session E. Verification Methodology Innovations:
Session Chair: Daniela Toneva (Intel)

E.1 *On the Development and Delivery of Configurable IPs.* Zijian Wang, Phong Phan and Baosheng Wang (AMD)
E.2 *SoC Verification Challenges Eased with Reusable Test Library and Performance Monitors*
Aravind Prakash, David Shan, and Hema Thyagarajan (NXP)
E.3 *Identifying Error-Prone Code and Coverage Holes*
Daniel Hansson (Verifyter, Sweden), Andreas Brytting (KTH Royal Institute of Technology, Sweden), and Markus Borg (RISE SICS AB, Sweden)
E.4: *Pain Points in Design Verification*
Gregory Kemp (SigTrak, United States)
E.5: *VCS Fine-Grained Parallelism Technology: Performance with Parallelism*
Wei-Hua Wan (Synopsys) and Sujit Shah (Centaur).

10:10-10:30 am - Coffee Break

10:30-11:30 am – PANEL 2:
Title: From Roll Your Own to Off the Shelf - The Changing World of FPGA Prototyping
Organizer: Harry Foster (Mentor Graphics)
Moderator: Kelly Larson (Paradigm Works)
Panelists:

1. Dave Schaefer (NXP)
2. Michael Becht (IBM)
3. Ram Narayan (ARM)
4. Steve Bailey (Mentor, A Siemens Business)
5. William Hodges (Intel)

11:30-12:10 am - Session F: Formal Verification
Session Chair: Himyanshu Anand (Nvidia)
F.1: *Formal Verification of a pipelined multiplier design for a high performance processor core*
Pratyush Jain (AMD)
F.2: *Formal Property Checking Applied to Microcontroller Low-Power Designs*
Alan Carlin (NXP), Tareq Altakrouri (Synopsys, United States), and Nemo Zhong (NXP)

12:10 - 1:00 pm - Lunch

1:00 – 1:20 pm – Invited Talk: Risk Analysis Based on Design Version Control Data
Raviv Gal, Avi Ziv, Gil Shurek and Giora Simchoni (IBM- Israel)
Session Chair: Atefeh Einafshar (Intel)

1:20-2:00 pm Session G: New Physical Design Verification Challenges
Session Chair: Xiao Sun (NXP)
G.1: SOC *Electromagnetic Crosstalk – Is it Real? Symptoms and Test cases*
Anand Raman, Yorgos Koutsoyannopoulos, Padelis Papadopoulos, Konstantis Daloukas, Thomas Flynn and Magdy Abadir (Helic)
G.2: *Meeting Aggressive Power, Performance and Area requirements of Automotive designs: Variation-Aware Timing Methodology*
Savithri Sundareswaran and Shruti Saxena (NXP)

2:00-2:45 pm - Session H. Embedded Tutorial
Session Chair: Wen Chen (NXP)
H.1: *The Application of Data Mining, Machine Learning & Big-Data Techniques in Functional Verification,* Eman El Mandouh and Ashraf Salem (Mentor,Egypt)

2:45-3:10 pm - Break

3:10-4:30 pm - Session I. Machine Learning:
Session Chair: Wen Chen (NXP)

I.1 *Machine Learning and Systems for the Next Generation of Formal Verification Tools*
Manish Pandey (Synopsys)
I.2 *Applying machine learning to verification at ARM*
Wade Walker (ARM)
I.3 *Automation of Processor Verification Using Recurrent Neural* Networks
Martin Fajcík (Brno University of Technology, Slovakia), Marcela Zachariášová and Pavel Smrž (Brno University of Technology, Czech Republic)
I.4 *Jamira (Justifiable Machine Reasoning Assistant) for Design Validation*
Joseph Skrovan and Amir Daneshbeh (Intel)

4:30-5:30 pm - Session J. Innovative Utilization of Standards
Session Chair: Adam Abadir (AMD)
J.1 *A Unified UVM Architecture for Flash-Based* Memory
Khaled Salah (Mentor Graphics, Egypt)
J.2 *Verification Prowess with the UVM Harness*
Jeff Vance, Jeff Montesano and Kevin Johnston (Verilab)
J.3 *TLM Virtual Platform for Fast and Accurate Power Estimation*
Magdy El-Moursy (Mentor Graphics, Egypt)

5:30 pm Closing Remarks – Magdy Abadir

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