# 17th International Workshop on Microprocessor and SOC Test and Verification

## Special Focus: Microelectronics Security Issues

## Final Program

December 12-13, 2016
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
**http://mtvcon.org**

General Chair: Magdy Abadir
Program Co-Chair: Jay Bhadra (NXP)
Program Co-Chair: Li-C. Wang (University of California at Santa Barbara)
Vice Program Chair: Wen Chen (NXP)

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# December 12, 2016

**7:30-8:00am: Registration and continental breakfast**

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**8:00 - 9:15 MTV Plenary Session**

**Opening Remarks: Magdy Abadir, MTV General Chair**

**Keynote Speaker** 1: **Dev Pradhan, Director of Global Automotive Engineering (NXP)**
Title: *Solving the Automotive Dilemma*
Organized by Synopsys

**Keynote Speaker 2: Debashis Chowdhury, VP of Engineering (Synopsys)**
Title: *The Future of Automotive: Verification Challenges and Solutions*
Organized by Synopsys

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**9:15-9:30 am - Coffee Break**

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**9:30-10:30 am - Session A. Verification Methodology Innovations**
**Session Chair: Daniela Toneva (Intel)**

**A.1** *From pre- to post-silicon and back - an ARM journey*
Merav Aharoni (IBM Research - Haifa, Israel)
**A.2** *SoC Fabric Verification Methodology*
Stefanos Homero Linakis, Alan Carlin and Linda Lin (NXP, Brazil & USA)
**A.3** *An Efficient Scenario Based Testing Methodology Using UVM*
Khaled Kabil, Amr Baher and Khaled Mohamed (Mentor Graphics, Egypt)

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**10:30-11:30 am - Session B. Memory Verification**

**Session Chair: Sankaranarayanan Gurumurthy (AMD)**

**B.1** *Fake CPU: A Flexible and Simulation Cost-Effective UVC for Testing Shared Caches,*
Saddam Quirem, Prasad Saravu (Samsung Austin R&D Center, USA)
**B.2** *Multi-Processor Memory Scoreboard: A multi-processor memory ordering and data consistency checker*, Prasad Saravu (Samsung Austin R&D Center, USA)
**B.3** *Formal Based Methodology For Inferring Memory Mapped Registers*
Haytham Saafan Shoukry (Mentor Graphics, Egypt), Mohamed Watheq El-Kharashi (Ain Shams University, Egypt), Ashraf Salem (Mentor Graphics, Egypt)

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**11:30- 11:55 am Invited pre-Lunch Speaker: Amol Bhinge, Sr. Verification Manager (NXP)**
*Title: SoC Design Verification: Challenges, Innovation and Beyond*
Organized by Synopsys
**Session Chair: Adam Abadir (AMD)**

**11:55 am-1:00 pm Lunch**

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**1:00-1:30 pm - Invited Speaker: Harry Foster, Mentor Graphics**
**Talk Title: *Trends in Functional Verification: A 2016 Industry Study***
**Session Chair: Adam Abadir (AMD)**

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**1:30-2:30 - PANEL Title: *The State of Functional Verification: Today and Tomorrow***
**Organizer and Moderator:** Harry Foster (Mentor Graphics)
**Panelists**:

1. Bill Greene (ARM)
2. Kelly Larson (Paradigm Works)
3. Ram Narayan (Oracle)
4. Neil Rosenberg (Intel)
5. Carmen Vargas (NXP)

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**2:30-3:00 pm - Break**

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**3:00-4:20 pm Session C. Test for IP Security and Trust**
**Session Chair: Wen Chen (NXP)**

**C.1** *Understanding security HWSW threats and mitigations*
Jean-Philippe Martin (Synopsys, USA)
**C.2** *Secure Outsourced IC Fabrication using Split Manufacturing*
Siddharth Garg (New York University, USA)
**C.3** *Towards Property Driven Hardware Synthesis*
Ryan Kastner (University of California, San Diego, USA)
**C.4** *SRAM-PUF Based on Selective Power-Up and Non-Destructive Scheme*
Mohd Syafiq Mispan, Basel Halak and Mark Zwolinski (University of Southampton, UK)

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**4:20-5:00 pm - Session D. Reliability**
**Session Chair: Li-C Wang (UCSB)**

**D.1** *A Case Study: Pre-Silicon SoC RAS Validation for NoC Server Processor*
Senwen Kan, Matthew Lam, Tyler Porter (AMD, USA), and Jennifer Dworak (Southern Methodist University, USA)
**D.2** *BTI Mitigation Technique Using Architectural Stress Balancing Data Patterns*
Haider Abbas, Mark Zwolinski, and Basel Halak (Southampton University, UK)

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**6:00pm - MTV Workshop Dinner**

**Venue:** *Fogo de Chão,* 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220.
Fogo de Chão is an authentic Brazilian steakhouse offering an incredible selection of grilled meats, salads and fresh vegetable. Please visit http://www.fogodechao.com/locations/austin/

**Transportation:** No transportation is provided. It is a short walk ~10-15 minutes from the Hyatt to the restaurant, or attendees can take a short taxi.

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# Tuesday December 13, 2016

**7:30-8:00 am - Registration and continental breakfast**

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**8:00-8:30 am Keynote Speaker: Prof. Mark Tehranipoor (University of Florida)**
Intel Charles E. Young Preeminence Endowed Professor in Cybersecurity
***Security Rule Check: A Closer Look at the Automated Test for Security***

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**8:30-9:50 am - Session E: IP Protection**
**Organizer: Mark Tehranipoor (University of Florida)**
**Session Chair: Sohrab Aftabjahani (Intel, USA)**

**E.1** *Hardware IP Protection: Past, Present and Future*
Jeyavijayan (JV) Rajendran (University of Texas at Dallas, USA)
**E.2** *Automatic RTL-to-Formal Code Converter for IP Security Formal Verification*
Xiaolong Guo, Raj Gautam Dutta (University of Central Florida, USA), Prabhat Mishra (University of Florida, USA), Yier Jin (University of Central Florida, USA)
**E.3** *Recent Trends in Intellectual Property (IP) Protection from Reverse Engineering*
Jae-Won Jang, Asmit De and Swaroop Ghosh (Penn State University, USA)
**E.4** *2.5D/3D Integration Technology for Enhancing Hardware Oriented Security and Trust*
Yang Xie, Chongxi Bao, Yuntao Liu and Ankur Srivastava (University of Maryland, USA)

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**9:50-10:10 am - Coffee Break**

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**10:10-11:10 pm - Session F: Security Assurance**
**Organizers: Sandip Ray and Wen Chen (NXP)**
**Session Chair: Sandip Ray (NXP)**

**F.1** *Hardware-based Workload Forensics & Malware Detection in Microprocessors*
Liwei Zhou and Yiorgos Makris (The University of Texas at Dallas, USA)
**F.2** *Tools and Development Environments for Hardware Security Assurance throughout Product Life Cycle: Past, Present, and Future* Seyed-Abdollah Sohrab Aftabjahani (Intel, USA)
**F.3** *Leveraging Simulation Environments for Security Verification*
Jason Oberg and Zachary Blair (Tortuga Logic, USA)

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**11:10-11:30 am - Invited Talk: Yehuda Naveh (IBM Research - Haifa Israel)**
*Performance Verification*

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**11:30-12:40 pm Lunch**

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**12:40-1:40 pm - Session G: Low power considerations**
**Session Chair: Xiao Sun (NXP)**

**G.1** *Transaction Level Power Modeling (TLPM) Methodology*
Magdy El-Moursy, Amr Baher and Mohamed Dessouky (Mentor Graphics, Egypt)
**G.2** *Verifying Low-Power Designs with Portable Stimulus*
Swami Venkatesan and Tom Anderson (Cadence, USA),
**G.3** *Low-power DFT Design for Effective Test Pattern Count and Test Time Reduction in a Custom High Performance ARM CPU Cluster*
Kelvin Ge (Samsung Austin R&D Center, USA)

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**1:40-2:40 pm - Session H: Test and DFT**
**Session Chair: Adam Abadir (AMD)**

**H.1** *Overcoming Tester Hardware Limitations in High Multisite Asynchronous Testing*
Stephanie Kirk, Ricardo Daniel Grande (Texas Instruments, USA)
**H.2** *Improving Stress Quality for Microprocessors using Faster-Than-At-Speed Functional Programs* Paolo Bernardi (Politecnico di Torino, Italy), Alberto Bosio (LIRMM, France), Riccardo Cantoro, Andrea Guerriero, Ernesto Sanchez, and Federico Venini (Politecnico di Torino, Italy)
**H.3** *Effective Speed Binning of Chip Designs by Mining Data From IDDQ Tests*
Louis Y.-Z. Lin, Denny C.-Y. Wu, and Charles H.-P. Wen (National Chiao Tung Univ., Taiwan)

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**2:40-3:00 pm Break**

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**3:00 pm-3:20 pm Invited Talk: Merav Aharoni (IBM Research - Haifa, Israel)**
*Combining simulation with formal verification to verify floating point divide and square-root*
Co-authored with Elena Blank (Intel, Israel)

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**3:20- 4:20pm Session I. Debug**
**Session Chair: Himyanshu Anand (nVidia, USA)**

**I.1** *Is the simulator wrong with my SystemVerilog code?*
Weihua Han (Synopsys, USA)
**I.2** *Automatic Debug with File Granularity*
Daniel Hansson and Patrik Granath (Verifyter, Sweden)
**I.3** *Tough Bugs Vs Smart Tools - L2/L3 Cache Verification using System Verilog, UVM and Verdi Transaction Debugging,* Vibarajan Viswanathan, Doug Reed (Centaur, USA), Juliet Runhaar and Jun Zhao (Synopsys, USA)

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**4:20 - 5:40 pm Session J. Verification Methodology Innovations**
**Session Chair: Galen Blake (Intel)**

**J.1** *Configuring a Date with a Model - A Guide to Configuration Objects and Register Models*
Jeffrey Montesano and Jeff Vance (Verilab, USA)
**J.2** *Coverage Closure Efficient UVM based Generic Verification Architecture for Flash Memory Controllers,* Ahmed Elyamany (Alexandria University, Egypt), Sameh Elashry (Ain-Shams University, Egypt), Amr Baher, Khaled Salah (Mentor Graphics, Egypt)
**J.3** *System Verilog Assertions Synthesis Based Compiler*
Omar Amin,, Youssef Ramzy, Omar Ibrahim, Ahmed Youssef (Alexandria University, Egypt), Khaled Salah, Haytham Shoukry and Mohamed Abdelsalam (Mentor Graphics, Egypt)
**J.4** *Scalable, Constrained Random Software driven Verification*,
Sainath Karlapalem, Shashank Venugopal (NXP Semiconductors, India) and Monica Farkash (NXP, USA)

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**5:40-5:50 pm Closing Remarks** – Magdy Abadir

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