15th International Workshop on Microprocessor Test and Verification Advance Program

December 15-17, 2014
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
http://mtvcon.org

General Chair: Magdy Abadir
Program Co-Chair: Jay Bhadra (Freescale Semiconductor Inc.)
Program Co-Chair: Li-C. Wang (University of California at Santa Barbara)

~~~~~~

Program Remarks

The technical program for MTV will take place on December 15 and 16th. The two day program offers an exciting array of papers, panels, invited talks and social activities.

On December the 17th, there are several activities planned jointly with the DVclub of Austin. All MTV attendees can attend those activities at no cost. Those acivities will take place in the Noris Conference Center, located in Anderson Lane North Austin which is about 10 miles way from the Downtown Hyatt and visitors from out town need to arrange their own transportation.

~~~~~~

Advanced Technical Program (schedule and contents subject to change)

December 15, 2014

7:30-8:00am: Registration and continental breakfast

~~~~~~

8:00 -8:10 Opening Remarks: Magdy Abadir, MTV General Chair

~~~~~~

8:10-8:45 am - Invited Talk
Threadmill: An Exerciser for Post-silicon Validation
Tom Kolan (IBM)

~~~~~~

8:45-10:05 am - Session A. Innovation in Best Practices
Session Chair: Li-C Wang (UC Santa Barbara)

A.1 *Improve the Verification Productivity: Some Best Practices from SoC and Processor Projects*
~~~~~~

Weihua Han (Synopsys)

A.2 *A case study of multi-processor bugs found using RIS generators and memory usage techniques*
Deepak Venkatesan and Pradeep Nagarajan (ARM)

A.3 *Fast Simulation of Pipeline in ASIP simulators*
Zdenek Prikryld (Brno University of Technology)

A.4 *Automatic UVM Environment Generation for Assertion-based and Functional Verification of SystemC Designs*
Michael Mefenza and Christophe Bobda (University of Arkansas)

~~~~~~
10:05-10:25am - Coffee Break
~~~~~~

10:25-11:30 am - ***PANEL 1:*** **Silk Road btw Emulation and Post Silicon**

Organizer and Moderator: Sean Sun (Freescale Semiconductor Inc.)

Participants:

- Farhan Rahman (AMD)
- Hillel Miller (Freescale Semiconductor Inc.)
- William Lindsay (Intel)
- Janick Bergeron (Synopsys)
- Al Czamara (Test Evolution)

~~~~~~
11:30-12:30 pm Lunch
~~~~~~

12:30-1:30pm - Session B. It Takes Hardware to Verify Hardware I
Session Chair: Shantanu Ganguly (Synopsys)

B.1 *Optimized Simulation Acceleration with Partial Testbench Evaluation*
Somnath Banerjee and Tushar Gupta (Mentor Graphics)

B.2 *Synthesizable Memory Models for Virtual prototyping*
Parikshit Dhodapkar (Open-Silicon)

B.3 *Hardware Synthesis from Software-oriented UML Descriptions*
Michele Lora, Francesco Martinelli and Franco Fummi (University of Verona)

~~~~~~

1:30-1:50pm - Invited Talk *HW/SW Debug in Simulation and Emulation Environment*
Shantanu Ganguly (Synopsys)

~~~~~~

1:50-2:50pm - Session C. Data Mining Applications in Verification and Test

Organizer: Nik Sumikawa (Freescale Semiconductor Inc.)
Session Chair: Wen Chen (Freescale Semiconductor Inc.)

C.1 *Harnessing data analytics toward coverage driven regression* (Invited Talk)
Raviv Gal, Einat Kermany, Avi Ziv (IBM)

C.2 *Automatic Assessment of Bimodality for Outlier Detection Application* (Invited Talk)
Keith Arnold (Optimal Plus)

C.3 *Data Mining in Functional Verification: Practical Results* (Invited Talk)
Monica Farkash (UT Austin)

~~~~~~

2:50-3:05pm Coffee Break

~~~~~~

3:05-4:25 pm: Session D. Mutation Analysis and Assertions
Session Chair: Alan Carlin (Freescale Semiconductor Inc.)

D.1 *Mutation based Feature Localization*
Jan Malburg, Emmanuelle Encrenaz and Goerschwin Fey (Universität Bremen)

D.2 *SystemVerilog Assertion Debugging based on Visualization, Simulation Results, and Mutation*
Moaz Mostafa, Mona Safar, Watheq El-Kharashi and Mohamed Dessouky (Mentor Graphics)

D.3 *A Novel Approach for SVA Generation of DDR Memory Protocols Based on TDML*
Mohamed Kayed, Mohamed Abdelsalam and Rafik Guindi (Mentor Graphics)

D.4 *JTAG-AXI debug IP with Performance meter mode*
Mrugesh Walimbe (Open-Silicon)

~~~~~~

4:25-5:25 pm - Session E. Special Session on Triage and Debug
Organizer: Eli Arbel (IBM)
Session Chair: Raviv Gal (IBM)

E.1 *Failure Triage, a Neglected Regression Debug Problem* (Invited Talk)
Zissis Poulos and Andreas Veneris (U of Toronto)

E.2 *Simulation Failure Triage and Debug in the Real World* (Invited Talk)
Bryan Hickerson, John Ludden and Michael Behm (IBM)

E.3 *Continuous Linting with Automatic Debug*
Daniel Hansson (Verfiyter)

~~~~~~

6:30pm - MTV Workshop Dinner

Venue: *Fogo de Chão,* 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220.
A short walk ~10-15 minutes from the Hyatt. Fogo de Chão is an authentic Brazilian steakhouse.
http://www.fogodechao.com/locations/austin/

Transportation: No transportation is provided. Attendees can take a short taxi or walk to the restaurant.

Tuesday December 16, 2014

7:30-8:00am - Registration and continental breakfast
~~~~~~

8:00-8:20 am - Invited Talk

Post-Silicon: The Next Frontier for EDA
Eric Rentschler (Mentor Graphics)

~~~~~~

8:20-9:20am - Panel 2. Sink, Swim, or Tread Water: Will current verification approaches scale to future challenges?
Moderator and Organizer: Harry Foster (Mentor Graphics)

Participants:

1. Alan Hunter (ARM)
2. Ram Narayan (Oracle)
3. Kelly Larson (Paradigm Works)

~~~~~~:
9:20-10:20 am - Session F. Stimulus Generation – A Smart Slot Machine
Session Chair: Robert Page (Freescale Semiconductor Inc.)

F.1 *A Random Instruction Sequence Generator for ARM Based Systems*
Shajid Thiruvathodi and Deepak Yeggina (ARM)

F.2 *LLVM based Random Test Program Generator for Samsung Reconfigurable Processor*
Jinsae Jung, Pankaj Shailendra Gode, Sukjin Kim, Narasinga Rao Miniskar, Jaehyun Kim and Shihwa Lee (Samsung)

F.3 *Directed Test Case Generation for x86 Instruction Decoding*
Peter-Michael Seidel (University of Hawaii)

~~~~~~
10:20-10:35 am - Coffee Break
~~~~~~

10:35-11:35am - Panel 3. Regression: Resource Blackhole
Organizer: Daniel Hansson, Verifyter

Moderator: Adam Abadir (AMD)

Participants:

- Daniel Hansson(Verifyter)
- Harry Foster (Mentor Graphics)
- JL Gray (Cadence)
- Olly Stephens (ARM)
- Fergus Casey (Synopsys ARC)
~~~~~~

~~~~~~

11:35-12:35 pm Lunch

~~~~~~

12:35-1:35pm - Session G. Formal Magic
Session Chair: Farhan Rahman (AMD)

G.1 *Using Formal Verification of Parameterized Systems in RAW Hazard Analysis in Microprocessors*
Lukas Charvat, Ales Smrcka and Tomas Vojnar (Brno University of Technology)

G.2 *A Case for Multi-level Combination of Theorem Proving and Model Checking*
Peter-Michael Seidel (University of Hawaii)

G.3 *'Dump what you need' – A Coverage Methodology to accelerate SoC Verification*
Ganesh Venkatakrishnan and Naresh Kadali (Open-Silicon)

~~~~~~

1:35-2:35 pm - Session H. Automatic Assertions Generation for complex designs
Organizer: Farhan Rahman (AMD)
Session Chair: Jay Bhadra (Freescale Semiconductor Inc.)

H.1 *Assertion Synthesis: Past, Present and Future.*
Yuan Lu (Atrenta):

H.2 *Auto Generation of Coverage Rich Assertions to Aid Emulation / Pre-Silicon*
Debjit Pal (AMD):

H.3 *Automated Assertions and Verification*
Tom Powell (Synopsys)

~~~~~~

2:35-3:00pm Coffee Break

~~~~~~

3:00-4:00pm - Session I. Innovative Memory Verification
Session Chair: Michael Hoyt (Paradigm Works)

I.1 *A configurable random instruction sequence (RIS) tool for memory coherence in multi-processor systems*
John Hudson, Bipin Ravi, Mark Dykes and Gunaranjan Kurucheti (ARM)

I.2 *Memory verification challenges solved*
Nasib Naser (Synopsys)

I.3 *FIES: A Fault Injection Framework for the Evaluation of Self-Tests for COTS-Based Safety-Critical Systems*
Andrea Höller, Gerhard Schönfelder, Nermin Kajtazovic, Tobias Rauter and Christian Kreiner (Graz University of Technology)

~~~~~~

4:00-4:20 - Invited Talk *Innovations in Hardware Assisted Verification – Enabling the Future of Verification*
Mike Stellfox (Cadence)

~~~~~~

4:20-5:20pm - Session J. It Takes Hardware to Verify Hardware II
Session Chair: Himyanshu Anand (Nvidia)

J.1 *Embracing the FPGA challenge for processor design verification*
Nitin Gupta and Chethan Harakchand (ARM)

J.2 *A FPGA Based Ecosystem for USBPHY Validation*
Maneesh Pandey, Shwetank Shekhar, Amit Sinha and Arun Mishra (Freescale Semiconductor Inc.)

J.3 *Virtual Platform for Embedded SoC Hardware and Software Codesign and Codebug*
Magdy El-Moursy, Ayman Sheirah, Mona Safar and Ashraf Salem (Mentor Graphics)

~~~~~~
5:20-5:25 pm Closing Remarks – Magdy Abadir
~~~~~~

Wednesday December 17, 2014

Venue:
Norris Conference Center, 2525 W Anderson Ln #365, Austin, TX 78757
(Please note the parking lot for the Conference Center is behind the left-hand side of the huge Wal-Mart)

Agenda:

11:30am: Doors Open / Networking

12:00pm: Lunch

- Keynote Presentation by Keith Sharp and Viresh Paruthi, IBM, "POWER8 Verification Advancements"

1:00pm: Networking

1:15-2:15pm: Tutorial 1

- Speaker Don Mills, sponsored by Sutherland HDL, "Synthesizing System Verilog: You Might Be Surprised at How Well Your ASIC or FPGA Synthesis Compiler Supports System Verilog!"

2:30-3:30pm: Tutorial 2

- Presenter TBD, sponsored by ARM, "Cache coherency in ARM multi-processing systems"
~~~~~~

MTV 2013 & 2014 CORPORATE SUPPORTERS