14th International Workshop on Microprocessor Test and Verification Final Program

December 11-13, 2013
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
http://mtvcon.org

General Chair: Magdy Abadir (Freescale Semiconductor)
Program Co-Chair: Jay Bhadra (Freescale Semiconductor)
Program Co-Chair: Li-C. Wang (University of California at Santa Barbara)

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Program Remarks

The technical program for MTV will take place on December 12 and 13th. The two day program offers an exciting array of papers, panels, invited talks and social activities.

On December the 11th, there are several activities done jointly with the DVclub of Austin. All MTV attendees can attend those activities at no cost.

Note that the activities of December the 11th will take place in North Austin which is about 10 miles way from the Downtown (no transportation provided).

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December 11, 2013

Venue: Norris Conference Center, 2525 W Anderson Ln #365, Austin, TX 78757

12:00 -1:00 pm: DVClub Speaker Luncheon
Registration : https://www.eventbrite.com/e/dvclub-soc-post-si-and-arm-debug-tickets-9507211325

SoC Verification
Amol Bhinge - Senior Verification Manager at Freescale Semiconductor

Post-Si Verification
Kevin Reick - System RAS Engineer at IBM

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1:15 – 2:15 pm Tutorial 1 – Cadence – Verification tutorial
Nick Heaton - Distinguished Engineer at Cadence Design Systems

2:30-3:30 pm Tutorial 2 – ARM Coresight IP tutorial for ARM debug architecture*
Paul Sigmon - Principal Application Engineer at ARM

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6-8pm: MTV Early Registration (For MTV registered attendees only).
Location Hyatt Lobby Area Bar
Meet the MTV organizers to pick-up your registration material, have a welcome drink and network.

Technical Program

December 12, 2013

7:30-8:00am: Registration and continental breakfast

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8:00-8:10 am: Plenary Session
Opening Remarks: Magdy Abadir, MTV General Chair (Freescale)

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8:10-9:10 am - Session A. Special Session on "Solving the Puzzles - Verification Constraint Solving"
Session Chair: Eyal Bin (IBM)

A.1 *Advanced Features in CSP for the Verification of Micro-processors* (Invited Talk)
Eyal Bin (IBM)

A.2 *On Coverage and Debug in Random Stimulus Generation* (Invited Talk)
Marat Teplitsky (Cadence)

A.3 *Efficiently Debugging Constraint Distributions and Performing Constraint What-If Analysis* (Invited Talk)
Alex Wakefield (Synopsys)

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9:10-10:10 am - Session B. Harvesting Time – Data Mining
Session Chair: Himyanshu Anand (NVIDIA)

B.1 *Leveraging Data feed Forward for higher Yield, better Quality and Test Time Reduction* (Invited Talk)
Eran Rousseau (Optimal Test)

B.2 *Applications of Data-mining for Test Cost Reduction and Quality Improvement* (Invited Talk)
Nik Sumikawa, Jeff Tikkanen, Li-C. Wang and Magdy Abadir (Freescale and UCSB)

B.3 *The Application of data mining techniques in processor and platform verification* (Invited Talk)
Wen Chen, Li-C Wang and Jay Bhadra (UCSB and Freescale)

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10:10-10:20 am - Coffee Break

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10:20-10:40 am - Invited Talk
Session Chair: Xiao (Sean) Sun (Freescale)

Mind the Gap: An Austin EDA Startup Story (Invited Talk)
Eric Hennenhoefer (ARM)

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10:40-11:40 am - *PANEL 1:* Time to Reduce SoC Verification Complexity – Really?

Moderator and Organizer: Xiao (Sean) Sun (Freescale)

Participants:

a. Alan Hunter (ARM)
b. J L Gray (Cadence)
c. Rowland Reed (Qualcomm)
d. Alex Johnson (Intel)
e. Paul Graykowski (Synopsys)

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11:40-12:30 pm Lunch

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12:30-1:30pm - Session C. Classic Tune in Functional Verification
Session Chair: Li-C. Wang (University of California, Santa Barbara)

C.1 *Functional Validation of a New Network Switch Architecture Using Rapid Prototyping Techniques*
Brian Kahne and Jim Holt (Freescale and Intel)

C.2 *Functional coverage based Random Test Program Generator (RTPG) comparison*
Vinayak Kamath, Farhan Rahman and Li-C Wang (AMD and UCSB)

C.3 *Modified Condition Decision Coverage: A Hardware Verification Perspective*
Mohamed Salem and Kerstin Eder (University of Bristol)

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1:30-2:50pm - Session D. New Frontier in Multimedia SoC verification
Session Chair: Hugo Cavalcanti (Freescale)

D.1 *Verification Methodology of Heterogeneous DSP+ARM Multicore processors in Multi-core System on Chip*
David Brier, Rama Venkatasubramanian, Sowmya Rangarajan and Abhishek Arun (Texas Instruments)

D.2 *Hierarchical Verification Framework for Samsung Reconfigurable Processor Video System*
Hoyoung Kim, Seonghun Jeong, Sunmin Kwon and Soojung Ryu (Samsung)

D.3 *Atom SOC Multimedia Verification Learnings*
Neeta Ganguly and Dan Fields (Intel)

D.4 *ARM Interconnect verification and performance analysis* (Invited Talk)
Nick Heaton (Cadence)

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2:50-3:00pm Coffee Break

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3:00-4:00pm - Panel 2. I Nailed Performance but Blew the Schedule!

Moderator and Organizer: Neill Mullinger (Synopsys)

Participants:
1. Tushar Mattu (Synopsys)
2. Bill Neifert (Carbon Design Systems)
3. Pete Wilson (Freescale)
4. Bernard Murphy (Atrenta)

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4:00-5:00 pm: Session E – Speeding Up Test and Debug
Session Chair: Jay Bhadra (Freescale)

E.1 *Measuring the Gain of Automatic Debug*
Daniel Hansson (Verifyter)

E.2 *Simulation debugging using on-the-fly design exploration*
Lior Altman, Avi Green, Paul Graykowski and Itai Yarom (The Hebrew University, Intel and Synopsys)

E.3 *MultiCore SOCs – Reusing tests* (Invited Talk)
Mark Kassab (Mentor Graphics)

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6:30pm - MTV Workshop Dinner

Venue: *Fogo de Chão,* 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220
A short (about 10 minutes) walk from Hyatt *Fogo de Chão* is located in downtown Austin. Fogo de Chão is an authentic Brazilian steakhouse. http://www.fogodechao.com/locations/austin/

Transportation: No transportation is provided. Attendees can take a short taxi or stroll to the restaurant.

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December 13, 2013

7:30-8:00am - Registration and continental breakfast
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8:00-8:30 am - Invited Talk
Session Chair: Harry Foster (Mentor Graphics)

Finding the Right Recipe: Designer-Level Verification with a Touch of Formal
Avigail Orni (IBM)

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8:30-9:30 am - Session F. Seek the Holy Grail - Emerging Verification Techniques
Session Chair: Nikolas Sumikawa (Freescale)

F.1 *Embedded Instrumentation: Opportunities for accelerating Design Verification* (Invited Talk)
Stephen Bailey (Mentor Graphics)

F.2 *Challenges in linking Emulation/Prototyping verification environments to simulation/formal* (Invited Talk)
Mike Stellfox (Cadence)

F.3 *Proving QBF-Hardness in Bounded Model Checking for Incomplete Designs*
Christian Miller, Christoph Scholl and Bernd Becker (University of Freiburg)

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9:30-9:40 am - Coffee Break
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9:40-11:00 am - Session G*:* Close the Backdoor - Security Test and Verification
Session Chair and Organizer: Jennifer Dworak (SMU)

G.1 *Preventing Security Leaks Using Formal Methods* (Invited Talk)
Chris Komar (Cadence)

G.2 *Verifying Authenticity and Trustworthiness of Integrated Circuits: Threats, Challenges, and Solutions* (Invited Talk)
Mark (Mohammad) Tehranipoor (UConn)

G.3 *Secure and Trusted SoC: Challenges and Emerging Solutions* (Invited Talk)
Swarup Bhunia (Case Western)

G.4 *Practical Security Validation* (Invited Talk)
Matthew King (Intel)

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11:00-11:50am - Panel 3: Hackers Not Welcomed - Security Verification Issues

Moderator and Organizer: Farhan Rahman (AMD)

Participants:

1. Ron Perez, (AMD)
2. Bill Schwarz (Freescale)
3. Chris Daverse (SRC)

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11:50-12:50pm - Lunch and Session H. Get the Big Picture - Advances in High-Level Modeling
Session Chair: Jing Huang (Freescale)

H.1 *Transaction Level Modeling – how this can speed up functional verification* (Invited Talk)
Phil Bishop (Cadence)
Presented by Mike Stellfox (Cadence)

H.2 *Ultra-Fast DMAC TLM Model for High Speed Virtual Platform Simulation*
Mona Safar, Magdy El-Moursy and Ashraf Salem (Ain-Shams University and Mentor Graphics)

H.3 *Communication Alternatives Exploration in Model-Driven Design of Networked Embedded Systems*
Emad Samuel Malki Ebeid, Franco Fummi and Davide Quaglia (University of Verona)

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12:50-1:50PM - Session J. Endless Challenges - Microprocessor Verification
Session Chair: Aseem Gupta (Freescale)

J.1 *State Retention Validation of C66x DSP core*
Rama Venkatasubramanian, Oluleye Olorode and Abhishek Arun (Texas Instruments)
Presented by David Brier (Texas Instruments)

J.2 *On the Functional Test of the Register Forwarding and Pipeline Interlocking Unit in Pipelined Processors*
Paolo Bernardi, Riccardo Cantoro, Lyl Ciganda, Boyang Du, Ernesto Sanchez, Matteo Sonza Reorda, Michelangelo Grosso and Oscar Ballan (Politecnico di Torino and STMicro)

J.3 *IP Testing for Heterogeneous SOCs*
Narendra Kamat (AMD)

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1:50-2:50pm - Panel 4 Kick a Notch Up – Spiced AMS Verification

Moderator and Organizer: Helene Thibieroz (Synopsys)

Participants:

1. Tom Barrett (Intel)
2. Dave Miller (Freescale)
3. Ron Shebel (Synopsys)
4. Amar Dwarka (Cadence)
5. Neil Spake (Freescale)
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2:50-3:00pm Coffee Break

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3:00-4:00Pm - Session K. Hardware Assisted Test and Debug
Session Chair: Adam Abadir (AMD)

K.1 *Memory verification in processor sub-systems* (Invited Talk)
Karen Darbinyan (Synopsys)

K.2 *Efficient way of multi-FPGA prototype for Samsung Reconfigurable processor*
Jinsae Jung, Sukjin Kim, Do-Hyung Kim and Shihwa Lee (Samsung)

K.3 *Dynamic Selection of Trace Signals for Post-Silicon Debug*
Kanad Basu, Prabhat Mishra, Priyadarsan Patra, Amir Nahir and Allon Adir (University of Florida, Synopsys, Intel and IBM)
Presented by Farimah Farahmandi (University of Florida, Synopsys)

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4:00-5:00pm - Session L. Reinforce Big Picture - ESL
Session Chair: David Kramer (Freescale)

L.1 *An Approach to Multi-core Functional Gate-level Simulation Minimizing Synchronization and Communication Overheads*
Tariq Ahmad and Maciej Ciesielski (University of Massachusetts, Amherst)

L.2 *Automatic Network Protocol Synthesis from UML Sequence Diagrams*
Emad Samuel Malki Ebeid, Franco Fummi, Francesco Stefanni and Davide Quaglia (University of Verona)

L.3 *Target Environment Simulation and its Impact on Architecture Validation: A Case Study of Thread-Level Speculative Execution*
Jack Mason and Gregory E. Simco (Nova Southeastern University)

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5:00 pm Closing Remarks – Magdy Abadir (Freescale)

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