12th International Workshop on Microprocessor Test and Verification Final Program

December 5-7, 2011
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
http://mtvcon.org

General Chair: Magdy Abadir (Freescale Semiconductor)
Program Co-Chair: Jay Bhadra (Freescale Semiconductor)
Program Co-Chair: Li-C. Wang (University of California at Santa Barbara)

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December 4, 2011

6:00-7:30pm: MTV Welcome and Early Registration
Location Hyatt Hill-Country-C room
Meet the MTV organizers to pick-up your registration material and network.

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Technical Program

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Day 1: December 5, 2011

7:30-7:50am: Registration and continental breakfast

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7:50-8:00am: Welcome and Opening Remarks by the Workshop General Chair: Magdy Abadir

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8:00-8:45am: Keynote: "Three decades of microcomputers in personal communications"
Mario A Rivas

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8:45-10:25am: High Level Verification
Session Chair: Neeta Ganguly (Intel)

A.1 *TLM Based Approach for Architecture Exploration of Multicore Systems-on-Chip*
*Mona Safar, Magdy El-Moursy, Ashraf Salem and Mohamed Abdelsalam (*Ain-Shams University, Mentor Graphics, Egypt)
A.2 *Verification of Parametrized RTL*
Xiushan Feng, Yinfang Lin and Jay Bhadra (Freescale, USA)
A.3 *Using Transaction Level Interface to Facilitate Communications between SystemVerilog – C/C++/SystemC*
Nasib Naser and Alex Wakefield (Synopsys, USA)
A.4 *A Unified Formal Framework for Analyzing Functional and Speed-path Properties*
*Oswaldo Olivo, *Sandip Ray, Jay Bhadra and Vivekananda Vedula (*University of Texas at Austin, Freescale, USA)

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10:25-10:40am Coffee Break

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10:40-11:55pm: SOC Verification
Session Chair: Sean (Xiao) Sun (Freescale)

B.1 *Questions to ponder for SOC validation*
Neeta Ganguly (Intel, USA)
B.2 *Verification Tests for MCAPI*
Alper Sen and Etem Deniz (Bogazici University, Turkey)
B.3 *An Efficient Overlapping Event Generation Method for Symmetric System Testing*
Devraj Kallappa Bakchowde and Nanda Kishore A. (Nokia Siemens Networks, India)

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12:00-1:00pm Lunch break

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1:00-2:40pm: Formal Methods
Session Chair: Alper Sen (Bogazici University, Turkey)

C.1 *Reusing of Properties after Discretization of Hybrid Automata*
Luigi Di Guglielmo, Franco Fummi and Graziano Pravadelli (Università di Verona, Italy)
C.2 *Bounded Model Checking of Incomplete Realtime Systems Using Quantified SMT Formulas*
Christian Miller, Karina Gitina and Bernd Becker (Albert-Ludwigs-University, Germany)
C.3 *Overview of Applying Reachability Analysis to Verifying a Physical Microprocessor*
Robert De B. Johnston and Ouiza Dahmoune (INRS-EMT, Canada)
C.4 *Transaction Based Sequential Equivalence Checking of High Level Designs against RTL*
Pankaj Chauhan, Anmol Mathur and Nikhil Sharma (Calypto, USA)

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2:40-3:00pm Coffee Break

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3:00-4:15 pm: Emulation/FPGA
Session Chair: T.-C. Lin (Cadence)

D.1 *Efficient way of ZeBu Flow deployment for a highly Configurable SoC*
Savitha H. Lakshminarayana (ARM, India)
D.2 *Model Checker to FPGA Prototype Communication Bottleneck Issue*
Ouiza Dahmoune and Robert De B. Johnston (INRS-EMT, Canada)
D.3 *Challenges and solutions for implementing embedded processor designs in multi-FPGA prototyping systems*
Juergen Jaeger (Cadence, USA)

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6:30pm MTV Workshop Dinner
Venue: *Fogo De Chao*, 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220
Description: A short (about 10 minutes) walk from Hyatt *Fogo De Chao* is located in downtown
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Austin. It features Brazilian cuisine with over 30 items including fresh cut vegetables, imported cheeses, cured meats and Brazilian side dishes. A wide variety of meat specialties expertly prepared by gaucho chefs and all you can eat gourmet salad and sides bar provides for a great experience amid stimulating discussions.

Transportation: Attendees can stroll to the restaurant or arrange for alternate ground transportation to the restaurant.

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Day 2: December 6, 2011

7:30-8:00am Registration and continental breakfast

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8:00-9:15am: Test
Session Chair: Vivek Vedula (Freescale)

E.1 *Overview on ATE Test and Debugging Methods for Asynchronous Circuits*
Christoph Wolf, Steffen Zeidler, Milos Krstic and Rolf Kraemer (IHP, Germany)
E.2 *Complexity Comparisons in Test Generation for Logic Circuits*
József Sziray (Széchenyi University, Hungary)
E.3 *Progressive-BackSpace: Efficient Predecessor Computation for Post-Silicon Debug*
Johnny J.W. Kuan and Tor M. Aamodt (University of British Columbia, Canada)

9:15-10:05am: Innovative Trends (Invited Session)
Session Chair: Vivek Vedula (Freescale)
F.1 *Functional Verification of Processor Virtualization*
Elena Tsanko and Yoav Katz (IBM, Israel)
F.2 *Applications of Datamining in Test and Verification*
*Nikolas Sumikawa, *Wen Chen, *Li-C. Wang, Jay Bhadra and Magdy Abadir (*University of California at Santa Barbara, Freescale, USA)

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10:05-10:20am Coffee Break

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10:20am-12:00pm Panel: SoC Verification Challenges and Solutions

Moderator: Eric Hennenhoefer (ARM)

Panelists:
Michael Stellfox (Cadence)
J L Gray (Verilab)
Hillel Miller (Freescale)
Alan Hunter (ARM)

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12:00-1:00pm Lunch break

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1:00-2:15pm: Static Timing and Clock Domain Crossing Analysis
Session Chair: Aaron Grenat (AMD)

G.1 *Achieving Glitch-Free Clock Domain Crossing Signals Using Formal Verification, Static Timing Analysis, and Sequential Equivalence Checking*

Kesava Talupuru and Sanjai Athi (MIPS, USA)
G.2 *A Full-chip Voltage and Clock-domain Crossing Sign-off Check Flow for Microprocessors*
Feng Gao, Suresh Chodisetti and Mahesh Sharma(AMD, USA)
G.3 *Automatic generation of software-based functional failing test for speed debug and on-silicon timing verification*
*Ernesto Sanchez, *Giovanni Squillero and +Alberto Tonda (*Politecnico di Torino, Italy; +Institut des Systèmes Complexes, France)

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2:15-3:30pm: Debug and SAT
Session Chair: Jing Zeng (MediaTek)

H.1 *Efficient Debugging of Multiple Design Errors*
Brian Keng, Duncan Exon Smith and Andreas Veneris (University of Toronto, Canada)
H.2 *Streamlining Debug with Protocol and Transaction Aware Debugging*
Paul Graykowski and Tareq Altakouri (Synopsys, USA)
H.3 *Improving Emulation Debugging Using Assertion Synthesis Technology*
Yuan Lu (NextOp, USA)

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3:30-3:45pm Coffee Break

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3:45-5:00pm: Low Power Verification
Session Chair: Alex Wakefield (Synopsys)

I.1 *High Coverage Power Integrity Verification in PSO Domains Employing Distributed PSO Switches*
Sergey Sofer, Asher Berkovitz and Valery Neiman (Freescale, Israel)
I.2 *A Test Method for Power Management of SoC-based Microprocessors*
Deacheol You, Young-Si Hwang, Youngho Ahn and Ki-Seok Chung (Hanyang University, Korea)
I.3 *Low Power Verification and Power Analysis with Emulation Systems*
Tsair-Chin Lin (Cadence, USA)

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5:00pm Closing Remarks – Magdy Abadir

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Day 3: December 7, 2011

Tutorials Day
(Free with MTV registration)

8:00-11:00am Tutorial: Optimally Addressing Verification Constraint Complexity for Effective Functional Convergence
Alex Wakefield and Shankar Hemmady (Synopsys USA)
Venue: Freescale Semiconductor Inc. 7700 W Parmer Lane, Building A, Room 150, Austin, TX 78729

Abstract:

As SoC design becomes larger and more complex, verification engineers are expanding constrained-random testing to meet the validation demand. This expansion creates a new set of challenges: engineers now face exponentially growing verification performance and capacity issues. It is no longer enough to write constraints that simply function to validate a design. Today, engineers must also optimize the constraints they write for performance if they wish to have any hope of both successfully validating their design and meeting their deadlines.
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In this tutorial, we discuss a scalable methodology for writing constraints and optimizing performance is which will improve engineers' productivity to write and debug ever-increasing amounts of larger, more complex sets of constraints. Our goal is to reduce the time needed for functional convergence, and later for debug and volume manufacturing. We will also discuss the vital role of Verification IP providers and users in this scenario.

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Free lunch at the Cool River Cafe (4001 West Parmer Lane, Austin, Texas 78727)

11:00am-1:30pm: DVClub presentation during lunch: "The Cortex-A15 Verification Story"

Bill Greene and Micah McDaniel (ARM USA)

Abstract:

This presentation will describe the advanced verification methodologies which are employed in the verification of Cortex-A15, including:

- Constrained random SystemVerilog unit level testbenches
- Coverage driven methodology utilizing black box and white box functional coverage for each unit
- Assertion based design where assertions are added by both verification engineers as well as RTL designers
- Top level (full CPU cluster) verification with multiple diverse random instruction generators, focusing on comprehensive ISA coverage and extensive stress of MP cache coherency
- System level (multiple CPU clusters + interconnect, memory controllers, graphics accelerators, other peripherals) emulation of the platform to enable booting of operating systems and running stress testing applications and workloads
- FPGA platforms to provide additional cost effective throughput

Details: http://www.dvclub.org/Events/Austin-The-Cortex-A15-Verification-Story

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