11th International Workshop on
Microprocessor Test and Verification Final Program

December 13-15, 2010
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
http://mtvcon.org

General Chair: Magdy Abadir (Freescale Semiconductor)
Program Co-Chair: Jay Bhadra (Freescale Semiconductor)
Program Co-Chair: Li-C. Wang (University of California at Santa Barbara)

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December 12, 2010

6-8pm: MTV Welcome Drink and Early Registration.
Location Hyatt Marker 10 Bar
Meet the MTV organizers to pick-up your registration material early while enjoying a complimentary drink.

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Technical Program

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Day 1: December 13, 2010

7:30-7:50am: Registration and continental breakfast
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7:50-8:00am: Welcome and Opening Remarks by the Workshop General Chair: Magdy Abadir (Freescale)
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8:00-9:40am: Debug
Session Chair: Jonathan Wolfe (Samsung)

A.1 *On the Resolution of Sequential Debugging*
Görschwin Fey, André Sülflow, and Rolf Drechsler (University of Bremen, Germany)
A.2 *An Automated Framework for Correction and Debug of PSL Assertions*
Brian Keng*, Sean Safarpour (Vennsa Technologies, Canada), Andreas Veneris*, (*University of Toronto, Canada)
A.3 *Post-silicon debugging with high level design descriptions and programmable controllers*
Masahiro Fujita, Bijan Alizadeh, Hiroaki Yoshida, Takeshi Matsumoto (University of Tokyo, Japan)
A.4 *Automation Techniques for Post-Silicon Debug of Timing Errors*
Azadeh Davoodi (University of Wisconsin at Madison, USA)

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9:40-10:30am: Architecture Validation
Session Chair: Eric Hennenhoefer (Obsidian)

B.1 *Using Software Architecture Patterns to Validate Performance of a Threaded Processor Architecture*

Jim Holt and David Lindberg (Freescale, USA)
B.2 *The impact a complete target environment simulation has on architecture validation: Case study of Speculative Execution Proposals*
Jack Mason (Nova Southeastern University, USA)
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10:30-10:45am Coffee Break
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10:45-12:00pm: Validation Test
Session Chair: Sean Sun (Mediatek)

C.1 *Fault Grading of Software-Based Self-Test procedures for Dependable Automotive Applications*
Paolo Bernardi, Ernesto Sanchez, Michelangelo Grosso, *Oscar Ballan and *Giovanni Fontana (politecnico di torino, Italy and *STMicroelectronics, Italy)
C.2 *Test Generation For Functional Verification of CMP Designs*
Padmaraj Singh and *David Landis (Nvidia, *Carnegie Mellon University, USA)
C.3 *A kernel based validation framework for functional test selection*
Po-Hsien Chang and Li-C Wang (University of California at Santa Barbara, USA)

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12:00-1:30pm Lunch break
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1:30-3:15pm Panel I: Verification is a problem, but is debug the root cause?

Moderator: Sean Safarpour (Vennsa Technologies)
Participants:
Alex Wakefield (Synopsys)
Bindesh Patel (Springsoft)
Harry Foster (Mentor Graphics)
Michael Stellfox (Cadence)

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3:15-3:30pm Coffee Break
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3:30 - 5:10 pm System Level
Session Chair: Steve Ravet (ARM)

D.1 *FPGA prototyping of the ARM Cortex A8 processor*
Steve Ravet (ARM, USA)
D.2 *Automatic Fault Localization for SystemC TLM Designs*
Hoang M. Le, Daniel Grosse and Rolf Drechsler (University of Bremen, Germany)
D.3 *Redesign and Verification of RTL IPs through RTL-to-TLM Abstraction and TLM Synthesis*
Nicola Bombieri, Franco Fummi, Valerio Guarnieri, Graziano Pravadelli and Sara Vinco (University of Verona, Italy)
D.4 *A Hardware/Software Co-design Framework using Abstract State Machines*
Nathan D. P. Buchanan and Hiren D. Patel (University of Waterloo, Canada)

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6:30pm MTV Workshop Dinner
Venue: *Fogo De Chao,* 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220
Description: A short (about 10 minutes) walk from Hyatt *Fogo De Chao* is located in downtown Austin. It features Brazilian cuisine with over 30 items including fresh cut vegetables, imported cheeses, cured meats and Brazilian side dishes. A wide variety of meat specialties expertly prepared by gaucho chefs and all you can eat gourmet salad and sides bar provides for a great experience amid

stimulating discussions.

Transportation: Attendees can stroll to the restaurant or arrange for alternate ground transportation to the restaurant.

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Day 2: December 14, 2010

7:30-8:00am Registration and continental breakfast

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8:00-9:15am: Formal Verification
Session Chair: Shaun Feng (AMD)

E.1 *An Embedded Reachability Analyzer And Invariant Checker (ERAIC)*
Ouiza Dahmoune and Robert de B. Johnston (INRS-EMT, Canada)
E.2 *Bounded Model Checking of Incomplete Networks of Timed Automata*
Christian Miller, Karina Gitina, Christoph Scholl and Bernd Becker (Albert-Ludwigs-Universitaet Freiburg, Germany)
E.3 *Schedulability Analysis for Multi-Core Global Scheduling under Cache Warm-Up Overheads based on Model Checking*
Wei Sheng, Yanyan Gao, Li Xi and Xuehai Zhou (University of Science and Technology, China)

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9:15-10:05am: Coverage
Session Chair: Srinagesh Loke (Qualcomm)

F.1 *Relational Database Schema for the UltraSparc Functional Coverage Flow*
James Roberts, Ray Voith and Michael Burns (Oracle, USA)
F.2 *Hi-Fi or One Small Music Library? Exploring the Implementation and Analysis Cost Trade-Offs of Coverage Model Design*
Paul Graykowski (Synopsys, USA) and Andrew Piziali (Independent Consultant, USA)

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10:05-10:20am Coffee Break
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10:20-12:00pm: SoC Verification
Session Chair: Sanjay Gupta (Freescale)

G.1 *An enhanced Strategy for Functional Stress Pattern Generation for System-on-Chip Reliability Characterization*
Mauricio de carvalho, Paolo Bernardi, Ernesto Sanchez and Matteo Sonza Reorda (Politecnico di Torino, Italy)
G.2 *System validation using IP-XACT standards*
Rajesh Chirumamilla (ARM, India)
G.3 *Using Graphics Processing Units for Logic Simulation of Electronic Desings*
Alper Sen, Baris Aksanli, Murat Bozkurt (Bogazici University,Turkey)
G.4 *An Efficient Event Generation Method for Testing a SOC with Multiple Processing Elements and Associated Peripherals*
Devraj Kallappa Bakchowde and Nanda Kishore A S (Nokia Siemens Networks India Pvt. Ltd, India)

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12:00-1:30pm Lunch break
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1:30-3:15pm Panel II: SystemVerilog Verification Methodology: Challenges and Solutions
Moderator: Alan Carlin (Freescale)

Participants:
Alan Hunter (ARM)
Janick Bergeron (Synopsys)
Mark Glasser (Mentor)
Sharon Rosenberg (Cadence)

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3:15-3:30pm Coffee Break
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3:30-4:45pm Invited Industry Session on Formal Methods for Power & Performance
Session Chair: Rajesh Raina (Freescale)

H.1 Ensuring Functional Integrity Under Aggressive Power and Performance Optimization
Pranav Ashar, CTO, Real Intent
H.2 Catching Performance Bugs Using Assertion Synthesis
Yushan Zhu, CEO, NextOp Software Inc.
H.3 Formal Verification as Fail-Safe for Advanced Power Management
Rajeev Ranjan, CTO, Jasper Design Automation

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4:45pm Closing Remarks – Magdy Abadir (Freescale)
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Day 3: December 15, 2010
Tutorials Day
(Free with MTV registration)
Venue: Freescale Semiconductor Inc.
7700 W Parmer Lane, Building A, Room 150, Austin, TX 78729

8:00-11:00am Tutorial: Experiences in Validating Power-Managed Processors and Wireless SoCs
Alan Hunter (ARM), Amit Kumar (CSR), and Prapanna Tiwari (Synopsys)

In this tutorial, we focus on the power management architecture verification experiences of Wireless SoCs and specifically focus on the tasks for validating a power managed ARM Cortex A-8 core and a power-managed GPS SoC.

The power management verification strategy was put in place with following goals in mind:
•Ensuring the intent of power-aware design is implemented per its architecture definition
•Correct sequencing of control signals during the switching and scaling of power supplies
•Correct input and output functionality of each power domain during the power cycles
•Coverage of all power states and all legal transitions between these power states

Some of the specific verification issues encountered and to be discussed here include the following:
•Ensuring that each of the domains are clamped correctly in all valid power states of the chip
•Ensuring level-shifters and level shifting clamps are correctly placed and validated for presence of different voltages and clock frequencies associated with the power domains
•Issues with voltages on level-shifters corrupting signals across domains
•Delay dependent issue with isolation resulting from voltage ramp times
•Un-initialized registers & memory contents on each power cycle corrupting downstream logic

We will review all of the key power management techniques and associated verification issues and then follow it up with the case studies of a processing core and a GPS chip.

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11:00am-1:30pm: DVClub presentation: "Topics in Verification Metrics"

Free lunch at the Cool River Cafe, Austin, TX

High Performance Collection of Coverage Metrics Using a Relational Database Backend
James Roberts (Oracle)

Abstract: A database is an ideal medium for collecting and analyzing coverage. At Oracle, we marry our Oracle database with coverage collection of our verification, and then use SQL to extract coverage metrics on-demand. This presentation outlines an intuitive scheme for database collection of coverage, and presents data showing the scalability and the high bandwidth this scheme is able to handle.

Using Bug Arrival Rates to Predict the Future
Greg Smith (Oracle)

Abstract: So much of today's metrics used to gauge the progress of a verification project are backwards looking – telling us what ground we have covered. In addition, many metrics commonly in use are subjective and prone to human errors of omission. This is a presentation on a different approach to design verification project metrics using bug arrivals to actually provide some predictive capability as well as aid in overall project planning.

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1:30pm-4:00pm: DVClub presentation: "Verification Tutorials I, II & III" Doug Smith (Doulos)

Details: http://www.dvclub.org/Events/Austin-Topics-in-Verification-Metrics
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