



10th International Workshop on Microprocessor Test and Verification

Final Program

December 7-9, 2009

Hyatt Regency Hotel, Austin, Texas, USA

Web Site: <http://mtvcon.org>

December 6, 2009

6-8pm: MTV Welcome Drink and Early Registration.

Location Hyatt Marker 10 Bar

Meet the MTV organizers to pick-up your registration material early while enjoying a complimentary drink.

Technical Program

Venue: Hyatt on Town Lake

Day 1: December 7, 2009

7:30-8:00am: Registration and continental breakfast

8:00-8:05am: Welcome and Opening Remarks by the Workshop General Chair: Magdy Abadir (Freescale)

8:05-9:45am

Session A: Architecture Verification

Chair: Mark Glass (ARM)

A.1 *A Methodology for Power-aware Pipelining via High-Level Performance Model Evaluations*

Luis Angel Bathen, Yongjin Ahn, Sudeep Pasricha* and Nikil Dutt (University of California Irvine and *Colorado State University)

A.2 *Simulation of a heterogeneous system at multiple levels of abstraction using Rendezvous based modeling*

Vyas Venkataraman, Di Wang, Wei Qin, Mrinal Bose* and Jayanta Bhadra* (Boston University, *Freescale).

A.3 *Fast Cycle Accurate Interpreted Simulation*

Zdenek Prikryl, Karel Masarik, Tomas Hruska and Adam Husar (Brno University of Technology, Czech Republic)

A.4 *The importance of full target environment simulation tests for architecture validation*

Jack Mason (Nova Southeastern University)

9:45-10:00am Coffee Break

10:00am-12:00noon

Session B: Verification issues for multi-core systems (invited session)

Organizer and chair: Sandip Ray (University of Texas at Austin)

B.1 System-level Performance Verification of Multicore Systems-on-Chip

Jim Holt, Jaideep Dastidar, David Lindberg, John Pape and Peng Yang (Freescale)

B.2 Dynamic Verification Methods for Message Passing Systems

Ganesh Gopalakrishnan (University of Utah)

B.3 Multiprocessor Architectures Don't Really Exist (But They Should)

Peter Sewell (University of Cambridge)

B.4 DPLL-based Reasoning in a Multi-Core Environment

Bernd Becker, Matthew Lewis* and Tobias Schubert (Albert-Ludwigs-University Freiburg, Germany and

*University of Freiburg, Germany)

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**12:00-1:30pm Lunch Break**  
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1:30-3:00pm

Panel: Top Three Verification Challenges

Moderator: Xiao Sun (Intel)

Panelists:

Shahram Salamian (Intel)

Bill Greene (Marvel)

Kelly Larson (MediaTek)

Rowland Reed (Qualcomm)

Jerry Vauk (AMD)

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**3:00-3:15pm Coffee Break**  
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3:15-4:05pm

Session C: Mutation Analysis

Chair: Eric Hennenhoefler (Obsidian)

C.1 Mutation Operators for Concurrent SystemC Designs

Alper Sen (Bogazici University, Turkey)

C.2 On the Mutation Analysis of SystemC TLM-2.0 Standard

Nicola Bombieri, Franco Fummi and Graziano Pravadelli (University of Verona, Italy)

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**4:05-5:20pm**

**Session D: Manufacturing Test**

**Chair: Jay Bhadra (Freescale)**

**D.1 Correlating System Test Fmax with Structural Test Fmax and Process Monitoring Measurements**

Chia-Ying (Janine) Chen, Jing Zeng\*, Li-C Wang and Jeff Rearick\* (University of California at Santa Barbara and \*AMD)

**D.2 Switch-Level Test Calculation for CMOS Circuits**

József Sziray (Széchenyi University, Hungary)

**D.3 A Path-Oriented Timing-Aware Diagnosis Methodology of At-Speed Transition Tests**

Jing Zeng, Jing Wang and Michael Mateja (AMD)

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6:30pm MTV Workshop Dinner

Venue: *Fogo De Chao*, 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220

Description: A short (about 10 minutes) walk from Hyatt *Fogo De Chao* is located in downtown Austin. It features Brazilian cuisine with over 30 items including fresh cut vegetables, imported

cheeses, cured meats and Brazilian side dishes. A wide variety of meat specialties expertly prepared by gaucho chefs and all you can eat gourmet salad and sides bar provides for a great experience amid stimulating discussions.

Transportation: Attendees can stroll to the restaurant or arrange for alternate ground transportation to the restaurant.

Day 2: December 8, 2009

7:30-8:00am Registration and continental breakfast

8:00-9:40am

Session E: Verification of Microprocessors and Complex IPs

Chair: Jawaid Iqbal (Intel)

E.1 *Mixing Simulated and Actual Hardware Devices to Validate Device Drivers in a Complex Embedded Platform*

Giovanni Perbellini, Franco Fummi*, Davide Quaglia*, Saul Saggin and Sara Vinco* (EDALab, *University of Verona, Italy)

E.2 *An ILP-based Diagnosis Framework for Multiple Open Defects*

Chen-Yuan (Ben) Kao, Chien-Hui (Christina) Liou and Charles H.-P. Wen (National Chiao Tung University, Taiwan)

E.3 *Verification of the QorIQ Communication Platform Containing CoreNet Fabric with SystemVerilog*

Robert Page and Sakar Jain (Freescale)

E.4 *Test Generation for Precise Interrupts on Out-of-Order Microprocessors*

Padmaraj Singh, David Landis* and Vijay Narayanan** (NVIDIA, *TTC and **Penn State University)

9:40-9:55am Coffee Break

9:55-12noon

Session F: Advanced Verification Techniques

Chair: Sanjay Gupta (ARM)

F.1 *Verification Methodologies to Facilitate Aggressive Power Reduction*

Sumit Ahuja and Sandeep Shukla (Virginia Tech)

F.2 *Symbolic Execution Engine to Explore Path Feasibility in Assembly Programs*

Subodh Sharma, Todd Dukes*, Jayanta Bhadra* and Ganesh Gopalakrishnan (University of Utah and *Freescale)

F.3 *Verification of Commercial Off The Shelf (COTS) System On Chips for use in Safety-Critical Applications*

David Beal*, Jason Lee, Rabi Mahapatra and Nikhil Gupta (*Virtutech and Texas A&M)

F.4 *Digital and Mixed-Signal Verification Differences*

James Lear (James Lear Consulting)

F.5 *Design of Efficient On-Chip Debugger for SoC*

Jingzhe Xu, Hyungbae Park and Jusung Park (Pusan National University, Korea)

12:00-1:30pm Lunch break

1:30-3:00pm

Panel: Role of Simulation-based verification in power managed designs

Moderator: I Bhanu Kapur (Mimasic)

Panelists:

Alan Hunter (ARM)

Jim Cleary (Intel)

Milind Padhye (Freescale)

Prapanna Tiwari (Synopsys)

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**3:00-3:15pm Coffee Break**

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3:15-4:55pm

Session G: Formal Verification

Chair: Roland Reed (Qualcomm)

G.1 *A Reconfigurable Five Stages Pipelined SAT Solver*

Mona Safar, Watheq El-Kharashi, Mohamed Shalan and Ashraf Salem* (Ain Shams University, Egypt and *Mentor Graphics)

G.2 *Using Backward Symbolic Justification to Constrain Initial State Don't-Cares in Model Checking*

Xiushan Feng, Brian McMinn, Richard Bartolotti and Mark Eslinger* (AMD and *Mentor Graphics)

G.3 *Induction-based Formal Verification of SystemC TLM Designs*

Daniel Grosse, Hoang M. Le and Rolf Drechsler (University of Bremen, Germany)

G.4 *Advance CPU verification using automatic detection of verification and specification gaps*

Sven Beyer (OneSpin Solutions GmbH, Germany)

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**4:55-5:45pm**

**Session H: Verification Management**

**Chair: Keith Savage (Centaur)**

**H.1** *Automating Verification Management*

Allan Cochrane and Alan Hunter (ARM)

**H.2** *Constraint Management and Checking in Template-Based Circuit Designs*

Richard Bartolotti, Tom Burd, Brian McMinn and Arun Chandra (AMD)

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5:45pm Closing Remarks – Magdy Abadir (Freescale)

Day 3: December 9, 2009
Tutorials Day
(Free with MTV registration)
Venue: Freescale Semiconductor Inc.

7700 W Parmer Lane, Building A Auditorium, Austin, TX 78729

8:00-11am: Tutorial 1

Using Rapid Prototyping for Microprocessor Design Verification

Neil Songcuan (Synopsys)

Abstract

The success of large-budget ASIC projects depends on the up-front choices made for their verification. Because of the increase in design complexity, speed, and large amounts of embedded software in today's designs, the choice of the hardware-assisted verification method to be used is more important than ever before. Join us for this technical hands-on tutorial as you will learn how rapid prototyping solves the challenges associated with traditional verification approaches and brings together all of the critical components into a complete and affordable solution that will enable you to find even the hardest-to-find hardware bugs, start software development earlier in the design cycle and integrate hardware and software well ahead of chip fabrication.

Summary

SoC design and verifications engineers, system validation engineers and software and firmware developers are encourage to attend this unique hands-on opportunity to directly work on a tightly integrated verification solution and flow that combines high-performance FPGA-based rapid prototyping hardware with industry standard implementation and debugging software.

To fully demonstrate how rapid prototyping is used for pre-silicon validation and software development, multiple laptops with pre-installed software and actual rapid prototyping boards will be available in a workshop lab environment. The tutorial is based on a synthesizable model of a 32-bit processor compliant with the SPARC V8 architecture and will guide users on how to take the design from implementation to full debug visibility.

The tutorial will first guide users on how to partition the 32-bit processor design into multiple FPGAs based on a targeted rapid prototyping hardware platform. The output of the partition result is FPGA-level projects which are then used as the input into an industry standard FPGA synthesis tool.

Prior to FPGA synthesis of the FPGA-level projects, users will be guided on how to instrument a design for debug visibility. Instrumentation allows users to define signals for triggering and modules for full design visibility using a technology called TotalRecall. TotalRecall allows for the first time, full design visibility of an FPGA-based rapid prototyping board at the RTL level while allowing the FPGA to run at real-time hardware speeds. This technology, when combined with assertion checkers, can be invaluable in pinpointing spurious, non-recurring, and other hard-to-locate corner case bugs in the design.

After design partitioning, instrumentation and synthesis are complete; users will then have the opportunity to setup and utilize the rapid prototyping board. The tutorial will guide users on the ease-of-use of setting up power, clock, and voltage regions available on the targeted rapid prototyping board and connect daughter boards based on standard connectors to interface with a memory module and basic input and output interfaces.

Since this tutorial is based on an embedded processor design, users will be guided to setup the rapid prototyping board through a standard JTAG interface with a software debugger application to monitor

the processor on-chip debug support unit. This setup allows for software development teams the capability to gain access to all memory and registers of the system, upload and execution of software as well as single-stepping, disassembly, and monitoring of on-chip bus traffic. Once the embedded processor software debugger has been established, engineers and software developers will essentially have an early pre-silicon platform on a high-performance rapid prototyping board to develop firmware and software applications of the ASIC design.

During the execution of a C program, users will enable the software debugger to monitor a set of trigger conditions for debug visibility of the design. If trigger conditions are met while running at real-time hardware speeds, the debugging tool will automatically create the hardware stimulus testbench (at the design block level) and guide users to their familiar software simulation environment for replay at the RTL level visibility leading up to the design bug. Software developers can then simply make the appropriate changes in the C program and reload into memory while the processor design continues to run on the rapid prototyping board. In essence, software and firmware engineers have a platform for early system validation and software development prior to chip fabrication.

After completing this unique hands-on tutorial, users will have a comprehensive understanding of how the different components of an integrated software and hardware solution fit together into a seamless debug flow, how TotalRecall enabled full design visibility at the RTL level, and the flexibility and ease of debugging hardware-captured stimulus in a standard software simulator environment.

12noon-1:30pm: Lunch Talk

DVClub (dvclub.org) lunch at the Cool River Cafe (4001 Parmer Lane, Austin, TX 78727)

Free lunch sponsored by the Austin chapter of DVClub.

Verification of the QorIQ Communication Platform's CoreNet Fabric with SystemVerilog

Sakar Jain and Robert Page (Freescale)

2:30-5:30pm: Tutorial 2

Why DFT, Design and Verification Teams must collaborate for efficient Silicon Debug

Nikhil Dakwala (Stringe Inc.)

Abstract

This tutorial demonstrates reasons for close collaboration between design, test, verification, ATE and fab teams, where it is needed and how to achieve it. We need to accept the fact that Silicon will fail. Therefore we must know how to debug failures, devise DFT to minimize most of them, and add strategic DFD for quick diagnosis. Multi-cores and non-discriminative ATPG algorithms almost always guarantee voltage droop problems on the tester, which means the chip designers need to consider Design for Debug (DFD) methods to combat droop and preserve test coverage. For example, unless constrained, all memory arrays can be accessed simultaneously during ATPG, which can severely stress ATE power supply.

Verification teams generate functional patterns to test critical paths and functionalities, which are impossible to create through ATPG tools. Hence these patterns need to be transferred to the tester and

debugged when they fail. For example, Memory BIST and patterns targeting paths going through memories and their controls can be fault graded, and their coverage used to augment global test coverage. When they fail on the tester, DFT, test and verification teams have to use their combined knowledge to quickly debug and resolve the fails.

Tutorial explains debug of failures across multiple dimensions of AC/DC speeds, voltage droop, No-Trouble-Found field returns and process variations. Tutorial demonstrates pattern debug directly on ATE, diagnostics and failure data-mining. Through case studies, Tutorial demonstrates the areas ripe for collaboration between design, test and verification teams. Tutorial details DFT and DFD solutions for quick resolution to failures and yield hits.
