9th International Workshop on Microprocessor Test and Verification Final Program

December 8-10, 2008
Hyatt Regency Hotel, Downtown Austin, Texas, USA
Web Site: http://mtv.ece.ucsb.edu/MTV/

December 7, 2008

6-8pm: Workshop Reception and registration at the Hyatt, Town Lake, Austin, TX

Technical Program

Hyatt Town Lake, Austin, TX

Day 1: December 8, 2007

7:30-8:00am: Registration and continental breakfast

8:00-8:10: Welcome and Opening Remarks by the Workshop General Chair: Magdy Abadir (Freescale)

8:10-9:50am
Session A: Memory consistency verification of shared memory multiprocessors
Session Chair: Jayanta Bhadra (Freescale)

A.1 *Black box and white box approaches to checking memory model compliance*
Chaiyasit Manovit*, Sudheendra Hangal** and Paul Loewenstein*** (*PwrLite, **Stanford, ***Sun)

A.2 *MP verification experience at AMD*
Jay Lyles (AMD)

A.3 *Testing Memory Models*
William W. Collier (Multiprocessor Diagnostics)

A.4 *Post silicon Memory Consistency validation of Intel Processors*
Chuck Fleckenstein and Stephan Zeisset (Intel)

9:50-10:15am: Coffee Break

10:15-11:30am
Session B: Post-silicon verification (invited session)
Session Chair: Sandip Ray (University of Texas at Austin)

B.1 *BackSpace: Moving Towards Reality*
F. M. De Paula, M. Gort, A. Hu, and S. J. E. Wilton (University of British Columbia Canada)

B.2 *Bridging Functional Verification and Post-Silicon Validation - The Coverage Aspect*
Avi Ziv (IBM)

B.3 *Effective pre-silicon verification for post-silicon validation - an Atom processor verification experience*
Shahram Salamian (Intel)

11:30-1:00pm: Lunch Break

1:00–3:00pm
Panel: *Standarizing on interoperability and methodology for verification - pro's and con's*
Moderator: Hillel Miller (Freescale)

Panelists:
Mike Stellfox (Cadence)
Kelly Larson (Mediatek)
J.L Gray (Verilab)
Robert Page (Freescale)
Harry Foster (Mentor)
Alan Hunter (ARM)

3:00-3:15pm: Coffee Break

3:15–4:30pm
Session C: SoC Test – I
Session Chair: Michael Bienek (AMD)

C.1 *A New Methodology for the Test of SoCs and for Analyzing Elusive Failures*
Alexander Weiss* and Christian Hochberger** (*Accemic Germany and **TU Dresden Germany)

C.2 *Noise-induced Timing Variation during At-Speed Delay Tests*
Jing Zeng, Jing Wang and Michael Mateja. (AMD)

C.3 *Silicon Debug of UltraSPARC T2 Post Burn-in Failure*
P. J. Tan, Patrick Fitzgerald, David Weisner, David Liu, and Scott Davidson (Sun Microsystems)

5:00–8:00pm
Dinner cruise and social event:
Dinner cruise on Town Lake aboard the Lone Star Boat
Boat departs in front of the Hyatt Hotel at 5pm sharp.

Day 2: December 9, 2008

7:30-8:00am: Registration and continental breakfast

8:00-9:40am
Session D: Advanced Verification Techniques – I
Session Chair: Sajosh Janarthanam (AMD)

D.1 *Preparing Rearchitected Designs for Sequential Equivalence Checking*
Mark Nodine (Intrinsity)

D.2 *Mining unreachable cross-timeframe state-pairs and its application on bounded sequential equivalence checking*
Lynn C.-L. Chang and Charles H.-P. Wen (National Chaio-Tung University Taiwan)

D.3 *Enhancing Sequential LEC Using a Cumulative Verification Methodology*
Nathan Sheeley, Nico Pena, Irfan Waheed and Mark Nodine (Intrinsity)

D.4 *Enhancing Verification Efficiency via Dynamically Focused, Selective and Intrusive Transactions*
Thinh Ngo (Mediatek Wireless Inc)

9:40-10:00am: Coffee Break

10:00-11:40am
Session E: Advanced verification techniques – II
Session Chair: Alper Sen (Freescale)

E.1 *AMD64 processor front-end verification (at unit-level testbench) with instruction set simulator*
Kana Murale, Scot Hildebrandt, Per Bojsen and Alfonso Urzua (AMD)

E.2 *Pre-silicon Verification Methodologies and Experiences of Intel's First MID Targeted SoC*
Barry Schneider. (Intel)

E.3 *Directed Random Verification for a Multiple GbE Network Processing SoC*
Janarthanan T Gilari and Xiao (Sean) Sun (Intel)

E.4 *Core Recovery Verification including Error Injection/Detection in IBM POWER Processors*
Chris Colletti and Brett St Onge (IBM)

11:40-1:00pm: Lunch Break

1:00–1:50pm
Session F: Low Power Verification
Session Chair: Jing Zing (AMD)

F.1 *Power Management Verification - an evolving discipline*
Ryan Pinto and James Cleary. (Intel)

F.2 *Applying Verification Collaterals For Accurate Power Estimation*
Sumit Ahuja, Deepak Mathaikutty* and Sandeep Shukla (Virginia Tech and *Intel)

1:50-2:40pm
Session G: SoC Test – II
Session Chair: Adam Abadir (AMD)

G.1 *Evaluation of Speed Path Identification of Structural Tests*
Jing Zeng*, Hsiu-Chuan Yu*, Jing Wang*, Michael Mateja*, Nicholas Callegari** and Li-C Wang** (*AMD and **University of California at Santa Barbara)

G.2 *A deterministic methodology for identifying functionally untestable path-delay faults in microprocessor cores*
Paolo Bernardi, Michelangelo Grosso, Ernesto Sanchez, and Matteo Sonza Reorda (Politecnico di Torino Italy)

2:40-3:30pm
Session H: Advances in formal verification
Session Chair: Liu Hanbing (AMD)

H.1 *Abstraction as a Practical Debugging Tool*
Sandip Ray (University of Texas at Austin)

H.2 *Property Analysis and Design Understanding in a Quality-Driven Bounded Model Checking Flow*
Ulrich Kuehne, Daniel Grosse, and Rolf Drechsler (University of Bremen Germany)

3:30-3:45pm: Coffee Break

3:45-5:15pm
Panel: ESL and Virtual Platform Verification – Debating Hardware, Software and Hybrid Solutions
Panel Organizer/Moderator: Magdy Abadir (Freescale)

Panelists:
Frank Schirrmeister (Synopsys)
Rodney Parrish (Cadence)
Hamendra Talesra (Coware)

Day 3: December 10, 2008

Tutorials Day
Location: Freescale Semiconductor Inc. Building B Auditorium
(7700 W Parmer Lane, Austin, TX 78729)

8:00-11am: Tutorial 1
SoC Power Management Verification and Testing Issues

Bhanu Kapoor (Mimasic), Manuel D'Abreu (SanDisk), Shireesh Verma (Conexant), Kaushik Roy (Purdue) and Marc Edwards (Synopsys)

We are at the crossroads of some fundamental changes that are taking place in the semiconductor industry. Power is a primary design criterion for bulk of the semiconductor designs now and a key reason behind the shift towards multi-core designs as increase in power consumption limits increases in clock speed at the rate we have seen in the past. Voltage is the strongest handle for managing chip power consumption. Dynamic power is proportional to the square of supply voltage and leakage power has a linear relationship with it. In addition, leakage power has an exponential relationship with the threshold voltage of the device. This implies that if voltage can be controlled to optimally meet the performance then there can be much to be gained in terms of powersavings.

In this tutorial, we look into the details of some of key power management techniques that leverage voltage as a handle: Power Gating (PG), Power Gating with Retention (RPG), Multiple Supply Voltages (MSV), Dynamic Voltage Scaling (DVS), Adaptive Voltage Scaling (AVS), Multi-Threshold CMOS (MTCMOS), and Active Body Bias (ABB). We look into their verification and testing implications. The use of above mentioned techniques also imply new challenges in validation of designs as new power states are created. We look into the characteristics of typical power states that exist in such designs and detail the techniques used in design validation. Techniques that leverage simulation, formal, and rule-based techniques are described in detail using examples. We make use of some of the latest mobile application-processor designs to aid explanation of these points. Power-aware testing is a major concern for designs that are leveraging voltage-based power management techniques and this poster will explore these challenges while providing some useful recommendations.

11:30am-2pm: Lunch Talk
DVClub (dvclub.org) lunch at the Cool River Cafe (4001 Parmer Lane, Austin, TX 78727)
Lunch sponsored by the Austin chapter of DVClub: Cadence, Doulos, Denali, Certess, Silicon Elite, Obsidian

Is it time to declare a verification war?
Brian Bailey

It is often said that verification is an art, but that has led us to statistics that show that success rates for chips are low. Perhaps it is time to think of it as war. In the words on Sun Tzu "If you know the enemy and know yourself, your victory will not stand in doubt". In this talk I will examine some of the fundamentals of verification and coverage and look at how far we may have strayed from the necessary understanding to win. In addition, some modern verification tools may be compounding those problems. Recent developments in the area of objective coverage measurement will be discussed along with the results of what may be a hot discussion at the Haifa Verification Conference this year.

2:30-5:30pm: Tutorial 2

Ensuring Functional Closure of a Multi-Core SoC Through Verification Planning, Implementation and Execution

Andrew Piziali, Shankar Hemmady (Synopsys), Alan Hunter (ARM), Kelly Larson (Mediatek) and Avi Ziv (IBM)

In a consumer electronics market that measures time from product conception to delivery in months and driven by seasonal sales cycles, first pass fully functional silicon is the ultimate determinant of product success. Functional verification remains the least predictable process in the design flow, largely due to the lack of a rigorous definition of the verification problem. A comprehensive verification plan derived from the product specification is the foundation of a metric driven process that quantifies the verification problem and defines its solution.

This tutorial addresses the verification of a modern multi-core SoC, having substantial software content, using such a quantitative approach. The student will learn how to analyze a specification to create a verification plan that describes the verification problem, quantifies it using measurable metrics, specifies the solution to the problem, and facilitates automation of functional closure. You will learn how to analyze a specification with an eye toward identifying product features and their associated attributes and behavioral requirements. Quantifying the verification problem through coverage model design is demystified. We describe how to choose the appropriate verification technique--ex. simulation, formal, hybrid--for each feature and design its application. Finally, the use of verification plan automation, allowing the verification plan to be used to directly control and measure the verification process is addressed.