Microprocessor Test and Verification Advance Program

December 5-6, 2007
Hyatt Town Lake Hotel, Austin, Texas, USA
Web Site: http://mtv.ece.ucsb.edu/MTV/

December 4, 2007

6-8pm: Workshop Reception and registration at the Hyatt, Town Lake, Austin, TX

Technical Program

December 5, 2007

7:30-8:00am: Registration and continental breakfast

8:00-9:15am
Session A: Simulation-Based Functional Verification of Simultaneous Multithreaded designs
Session Chair: Michal Rimon (IBM)

A.1 *Validation of Simultaneous Multi-Threading Designs*
David Burns (Intel)

A.2 *Verification Methodology of a Highly Threaded Sun UltraSPARC T2 Server-On-Chip*
Ajay Nath, Jai Kumar, and David Wilkins (Sun)

A.3 *Simultaneous Multi-Threading Verification of the POWER5 and POWER6 High Performance Processors*
John Ludden (IBM)

9:15-9:30am: Coffee Break

9:30–10:45am
Session B: Power Modeling and Estimation
Session Chair: Kamal Khouri (Freescale)

B.1 Assertion-based Modal Power Estimation
*Sumit Ahuja, Deepak A. Mathaikutty, Sandeep Shukla, and Ajit Dingankar** (Virginia Tech and *Intel USA)

B.2 Early Models for System-level Power Estimation
Dam Sunwoo, Hassan Al-Sukhni, Jim Holt*, and Derek Chiou* (U Texas Austin and *Freescale)

B.3 Trends in Design and Verification of Low Power SOCs
Srikanth Jadcherla (Synopsys)

10:45am–12pm
Session C: Industrial Verification Applications
Session Chair:

C.1 Intel® First Ever Converged Core Functional Validation Experience: Challenges, Methodologies, Results and Learning
Tommy Bojan, Igor Frumkin, and Robert Mauri (Intel, Israel & USA)

C.2 Automotive Microcontroller End-of-Line Test via Software-based Methodology
W. Di Palma, D. Ravotto, E. Sanchez, M. Schillaci, M. Sonza Reorda, and G. Squillero* (Politecnico di Torino and *Magneti Marelli, Italy)

C.3 Formal Verification in IP/SoC Verification Methodology
Rekha Bangalore, Jason Castillo, and Joseph Fernando (Freescale)

12-1:00pm: Lunch Break

1:00–2:15pm
Session D: Silicon Debug
Session Chair: Michael Bienek (AMD)

D.1 Impact of Temperature Inversion on Timing Sign-off and Design Methodology
Sean Wu+, Alex Tetelbaum+, Pouria Bastani*, and Li-C. Wang** (*UC Santa Barbara and +LSI)

D.2 Evaluation of Speed Path Identification of Structural Tests
Jing Zeng, Michael Mateja, Jing Wang, Nicholas A. Callegari, and Li-C. Wang** (AMD and *U California Santa Barbara)

D.3 Failure Analysis of Silicon using Formal Verification Techniques
Noah Bamford, Eric Chapman, and Rekha Bangalore (Freescale)

2:15–3:55pm
Session E: Verification Methodology
Session Chair: Mark Gillman (Denali)

E.1 *Unique Methodologies to Find Those Elusive Bugs*
Michael Chen (Mentor)

E.2 Mining simulation traces and its applications in functional verification
Onur Guzey and Li-C. Wang **(**U California Santa Barbara)

E.3 Top Level SOC Interconnectivity Verification using Formal Techniques
Subir Roy (TI, India)

E.4 Chico: An OnChip Hardware Checker for Pipeline Control Logic
Andrew DeOrio, Adam Bauserman, and Valeria Bertacco (U Michigan)

4:15–9:00pm
Dinner and social event:

- *Duck Tour* of Austin (touring Austin's historic downtown, Town Lake, and around town)
- Dinner and Live Music at Belmont Restaurant in downtown Austin
- Optional bar hopping from 9pm onward

Bus departs from Hyatt at 4:15pm sharp.

December 6, 2007

7:30-8:00am: Registration and continental breakfast

8:00-9:15am
Session F: Advanced Specification and Verification
Session Chair: Brad Perdue (Coware)

F.1 Runtime Verification of k-Mutual Exclusion for SoCs
*Selma Ikiz and Alper Mehmet Sen** (U Texas Austin and *Freescale)

F.2 A Scalable Symbolic Simulator for Verilog RTL
Sasidhar Sunkari, Supratik Chakraborty, Vivekananda Vedula, Kailasnath Maneparambil*** (Intel, India, *Indian Institute of Technology Bombay, India and **Intel, US)

F.3 An ADL for Functional Specification of IA32
Wei Qin, Asa Ben-Tzur, and Boris Gutkovich** (Boston U and *Intel Israel)

9:15-9:30am: Coffee Break

9:30–10:45am
Session G: Formal Verification
Session Chair: Amrish Chokhavatia (Synopsys)

G.1 Mechanized Certification of Secure Hardware Designs
Sandip Ray and Warren Hunt (U Texas Austin)

G.2 Application of Lifting in Partial Design Analysis
Marc Herbstritt, Vanessa Struve, and Bernd Becker (Albert-Ludwigs-University, Germany)

G.3 Model-checking based Verification for Hardware Designs specified using Bluespec System Verilog
Gaurav Singh and Sandeep K. Shukla (Virginia Tech)

10:45am–12pm
Session H: Yield Analysis and Test Applications
Session Chair: Sean Sun (Intel)

H.1 Embedded Tutorial: Recent Advances in Yield Analysis
Al Crouch (Innovys)

H.2 Verification of Gate Level Model for Custom Design in Scan Mode
Baker Mohammad, Geewhun Seok, Hong Kim, and Paul Bassett (Qualcomm and U Texas Austin)

H.3 Reduction of Power Dissipation during Scan Testing by Test Vector Ordering
*W.-D. Tseng and L.-J. Lee** (U Yuan Ze, Taiwan and *National Army Academy, Taiwan)

12-1:00pm: Lunch Break

1:00–3:00pm
Panel: IP vs SOC verification: where one ends and the other begins
Moderator: Eric Hennenhoefer
Organizers: Jay Bhadra, Magdy Abadir (Freescale) and Eric Hennenhoefer (Obsidian)

Participants:
Ken Albin (AMD)
Harry Foster (Mentor)
Nari Krishnamurthy (Nusym Technology)
Kelly Larson (Analog Devices)
Micah McDaniel (ARM)
Hillel Miller (Freescale)
Mike Pedneau (TI)
Mike Stafford (IBM)

3:00–3:50pm
Session I: Analog/Mixed-signal Verification
Session Chair: Alper Mehmet Sen (Freescale)

I.1 Application of Automated Model Generation Techniques to Analog/Mixed Signal Circuits
Scott Little, Alper Mehmet Sen, and Chris Myers* (U Utah and *Freescale)

I.2 Mixed signal Verification
John Pierce and Abhijeet Kolpekwar (Cadence)

3:50–4:00pm: Coffee Break

4:00–5:15pm
Session J: Test and Testbench Generation
Session Chair: Adam Abadir (AMD)

J.1 Automatic Testbench Generation for Rearchitected Designs
Mark Nodine (Intrinsity)

J.2 A CLP-based Functional ATPG for Extended FSMs
Franco Fummi, Ian G. Harris, Cristina Marconcini, and Graziano Pravadelli* (Universit `a di Verona and *U California Irvine)

J.3 On Automatic Test Block Generation for Peripheral Testing in SoCs via Dynamic FSMs Extraction
D. Ravotto, E. Sanchez, M. Schillaci, M. Sonza Reorda, and G. Squillero (Politecnico di Torino, Italy)

5:15pm – Closing Remarks
