Call For Participation:

IEEE 6th International Workshop on Microprocessor Test & Verification (MTV 2005)
Hyatt Town Lake Hotel, Austin, Texas, USA
November 3-4, 2005

Web Site: http://mtv.ece.ucsb.edu/MTV/

Deadlines:
- Advance Workshop Reservation: October 23, 2005, 5pm USA EST
- Advance Hotel Registration: October 12, 2005 Rate $149

MTV'05 Workshop Registration and Hotel Reservation are available at
http://mtv.ece.ucsb.edu/MTV/

Hyatt Town Lake Hotel, 208 Barton Springs Road, Austin, Texas 78704
Reservation Number: 1 (800) 233-1234 or (512) 477-1234

Final Program
MTV 2005

Wednesday, November 2, 2005
7-9pm: Pre-event Reception at the Hyatt, Town Lake, Austin

Thursday, November 3, 2005
7:30-8:30am: Continental Breakfast

8:30-8:40am: Opening Introduction, Magdy Abadir, General Chair

8:40-10:45am
Session A: Architecture Description Languages,
Organizer: Eli Almog, IBM,
Session Chair: Magdy Abadir, Freescale Semiconductor
A.1 A Study of Architecture Description Languages from a Model-based Perspective
Prof. Wei Qin, Boston University, Sharad Malik, Princeton University.

A.2 An Introduction to the Plasma Language, Brian Kahne, Pete Wilson, Freescale Semiconductor, Aseem Gupta and Nikil Dutt, University of California at Irvine.

A.3 Embedded Processor Design and SW Tool Generation Using LISA, Andreas Hoffmann, CoWare.

A.4 Verifying Configurable ISAs Described in Tensilica's Instruction Extension (TIE) Language, Dhanendra Jani, Tensilica

A.5 Processor Architecture Description Language for Test Generation, Eli Almog, IBM.

10:45am-11:00am: Coffee Break

11am – 11:50am
Session B: SAT Applications
Session Chair: TBD

B.1 Bounded Invariant Checking of Partial Implementations Using a Structural SAT-Solver, Marc Herbstritt and Bernd Becker, Albert-Ludwigs-University of Freiburg, Freiburg, Germany

B.2 PaMira – a Parallel SAT Solver with Knowledge Sharing, Tobias Schubert, Matthew Lewis, and Bernd Becker, Albert-Ludwigs-University of Freiburg, Freiburg, Germany

11:50am-1pm: Lunch Break

1pm – 2:40pm
Session C: Debug and Diagnosis
Session Chair: Li-C Wang, UC-Santa Barbara

C.1 Diagnosing faulty functional units in processors by using automatically generated test sets, P. Bernardi, E. Sanchez, M. Schillaci, G. Squillero, M. Sonza Reorda
Dipartimento di Automatica e Informatica, Politecnico di Torino, Italy

C.2 Post-Verification Debugging of Hierarchical Designs, Moayad Fahim Ali, Sean Safarpour, Andreas Veneris, University of Toronto, Magdy S. Abadir, Freescale Semiconductor, and Rolf Drechsler, University of Bremen, Germany

C.3 An Investigation of Excitation Balance and Additional Mandatory Conditions for the Diagnosis of Fortuitously Detected Defects, Jennifer Lynn Dworak, Brown University
C.4 Exploiting an I-IP for both Test and Silicon Debug of Microprocessor Cores, P. Bernardi, M. Grosso, M. Rebaudengo, M. Sonza Reorda, Politecnico di Torino, Dipartimento di Automatica e Informatica, Torino, Italy

2:40 – 3pm: Coffee Break

3:00 – 5:05pm

Session D: Functional Test Generation, Circuit Marginality and Speed Binning
Session Chair: TBD

D.1 Is IDDQ Test of Microprocessors Feasible? Bin Xue and D. M. H. Walker, Texas A&M University

D.2 Improved methods for Circuit Marginality, Speed Path & Manufacturing Defect Detection, Greg Czajkowski, Dave LaFollette, and Paul R. Zehr, Intel Corporation

D.3 System Level Verification using Hierarchical Test Case Synthesis, Adnan Hamid, Breker Verification Systems

D.4 The Generator Construction Set -- A New Approach to Random Test Generators, Melanie D. Typaldos and Rebecca Cavanaugh, Obsidian Software Inc.

D.5 Simulation Data Mining for Functional TPG, Charles H-P Wen and Li-C. Wang, UC-Santa Barbara

5:30-9 pm: Dinner and Social Event

November 4, Friday

7:30 – 8:30am: Continental Breakfast

8:30am – 10:10am

Session E: IP and Processor Validation
Session Chair: TBD

E.1 Automated Extraction of Structural Information from SystemC based IP for Validation, David Berner, Institut de Recherche en Informatique et Syst`emes Al´eatoires, France Hiren D. Patel, Deepak A. Mathaikutty, and Sandeep K. Shukla, Virginia Polytechnic and State University
E.2  
Pre-Silicon Validation of IPF Memory Ordering for Multi-Core Processors, Soohong Kim, Intel Corporation

E.3  
Automatic Generation of High Performance Embedded Memory Models for PowerPC Microprocessors, Jayanta Bhadra, Magdy S. Abadir, David Burgess, and Ekaterina Trofimova, Freescale Semiconductor

E.4  
Language-driven Validation of Pipelined Processors using Satisfiability Solvers, Prabhat Mishra, Heon-Mo Koo, and Zhuo Huang, University of Florida, Gainesville, Florida

10:10am – 10:20am: Coffee Break

10:20am – 12noon

Session F: High-level ATPG and Verification
Session Chair: Magdy Abadir, Freescale Semiconductor

F.1  
On PSL Properties Re-use in SoC Design Flow Based on Transaction Level Modeling, Nicola Bombieri, Andrea Fedeli, STMicroelectronics, and Franco Fummi, University of Verona

F.2  
A Pseudo-Deterministic Functional ATPG based on EFSTM Traversing, G. Di Guglielmo F. Fummi C. Marconcini G. Pravadelli, Dipartimento di Informatica - Università di Verona, Italy

F.3  
Search-space optimizations for high-speed ATPG, Jorge Campos and Hussain Al-Asaad, University of California, at Davis

F.4  
HW/SW Co-Verification of a RISC CPU using Bounded Model Checking, Daniel Grosse, Ulrich Kuehne, Rolf Drechsler, University of Bremen

12:00 – 1:15pm: Lunch Break

1:15 – 2:30pm

Session G: Invited Presentations
Session Chair: Madhusudan S Ponnada, Intel Corporation

G.1  
3D circuits and its test challenges, T. M. Mak, Intel Corporation

G.2  
Equivalence Checking -- An Industry Perspective, Kei-Yong Khoo, Cadence Design Systems, Inc.

G.3  
A TDM Test Scheduling Method for Network-on-Chip Systems, Mark Nolen, Rabi Mahapatra and Ray Mercer, Texas A&M University
2:30pm-3:45pm

**Special session H: Advanced Industrial Developments in Test**
*Organizer: Al Crouch, Inovys*
*Session Chair: TBD*

Speaker: Jason Doege, Cadence  
Speaker: Bill Bruce, Silicon Aid  
Speaker: Al Crouch, Inovys

3:45-4:00pm Coffee Break

4:00 – 5:15pm

**Special session I: Sequential Equivalence Checking**
*Organizer/Session Chair: Anmol Mathur, Calypto Design Systems*

**I.1** Using *sequential equivalence checking in a microprocessor design flow*, Brian Kahne and Magdy Abadir, Freescale Semiconductor

**I.2** *Sequential Equivalence Checking of RTL Models*, Gagan Hasteer, Venkat Krishnaswamy and Nikhil Sharma, Calypto Design Systems

**I.3** *Seq-SAT - An Efficient Sequential Circuit SAT Solver and Its Application to Sequential Equivalence Checking*, Feng Lu, K.-T. Cheng and L.C Wang, Department of ECE, University of California at Santa Barbara

5:15pm --- **Closing Remarks (committee meeting)**