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Journal of Electronic Testing: Theory and Applications (JETTA) Special Issue on Verification and Testing Challenges in Future Microprocessor and SoC Designs

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Aims and Scope

With increasing sophistication of VLSI technology, process, and architecture, microprocessors and SoC systems continue to increase in complexity. This has resulted in an increasing trend in design errors, manufacturing flaws, and security holes in modern VLSI systems. The situation will be exacerbated in future systems with increasingly smaller form factors, higher integration complexity, and more complex manufacturing process. Consequently, verification and testing technology will continue to dominate as crucial factors in time-to-market, reliability, and cost of VLSI systems. There has been significant research on verification and testing challenges and their synergy for modern and future VLSI systems. However, much of the research is scattered across different conference proceedings and journal issues, and entail different (and often conflicting) approaches, formalisms, and assumptions. It is time to provide a focused and unified look at the domain, identify and consolidate the key problems and emerging trends in test and verification, and reflect on how to apply the techniques synergistically for ensuring reliability of current and future systems.

The special issue of *Journal of Electronic Testing: Theory and Applications (JETTA)* will focus on Verification and Testing Challenges with Future VLSI Systems, and some of the approaches taken to mitigate these challenges. The goal is to provide a unified reference for trends in verification and testing research. Topics of interest include, but are not limited to, the following.

- Validation of microprocessors and SOCs
- Experiences on test and verification of high performance processors and SOCs
- High-level test generation for functional verification
- Emulation techniques
- Silicon debugging
- Low Power verification
- Formal techniques and their applications
- Verification coverage
- Test generation at the transistor level
- ESL Methodology
- Virtual Platforms
- Software verification
- Circuit level verification
- Switch-level circuit modeling
- Timing verification techniques
- Design error models
- Design for testability or verifiability
- Optimizing SAT procedures for application to testing and formal verification

Papers disseminating research with a strong vision for future trends in verification and testing are particularly welcome. (Note, however, that the papers must describe technical research and not just position statements.) Research exploiting synergy between different test or verification techniques is encouraged.

Submission Procedure

Papers should be written in general term understandable by the usual audience of the journal. The work must not have been published before; substantial extensions of previously published conference papers is permitted, but the corresponding conference papers must be cited along with a discussion on the nature of extension and novel contributions in the current submission. In particuar, expanded versions of manuscripts from submissions to MTV 2011 (`http://mtvcon.org`) are welcome, but the papers must be elaborated to include details as expected from a journal publication. Concurrent submission to any other conference or journal is a ground for rejection without review. All papers will be fully refereed to ensure conformance with the regular journal standards. Since a key objective is to provide a comprehensive reference for the different research challenges and progress made in the area, a detailed discussion of related research is expected.

Authors should submit papers through the Web site `www.editorialmanager.com/jetta`, specifying the article type as "SI: VTMSOC". Submissions should be formatted according to author guidelines available at `http://www.springer.com/10836`.

Important Dates

Paper Submission:	March 25, 2013
Notification:	July 22, 2013
Camera-ready Version:	August 23, 2013

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